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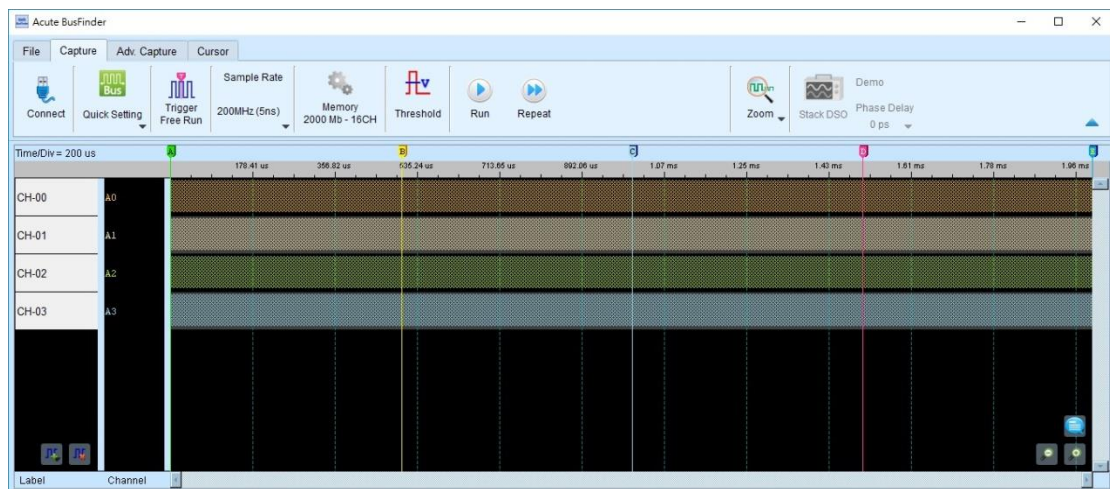
Chapter 1 Bus Decode

Basic operation

Add a Bus Decode

Method 1:

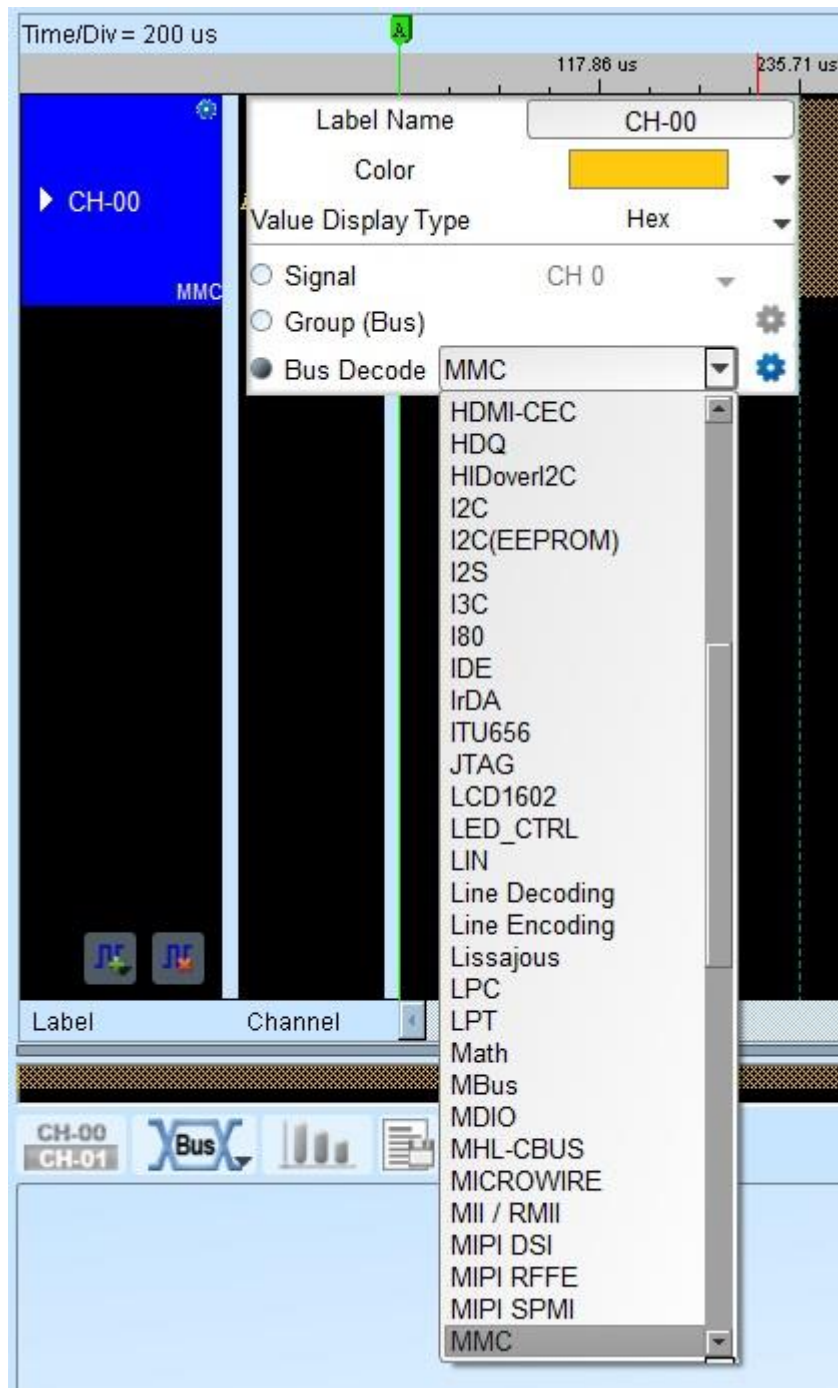
Click the wizard in the menu, and select the bus decode.



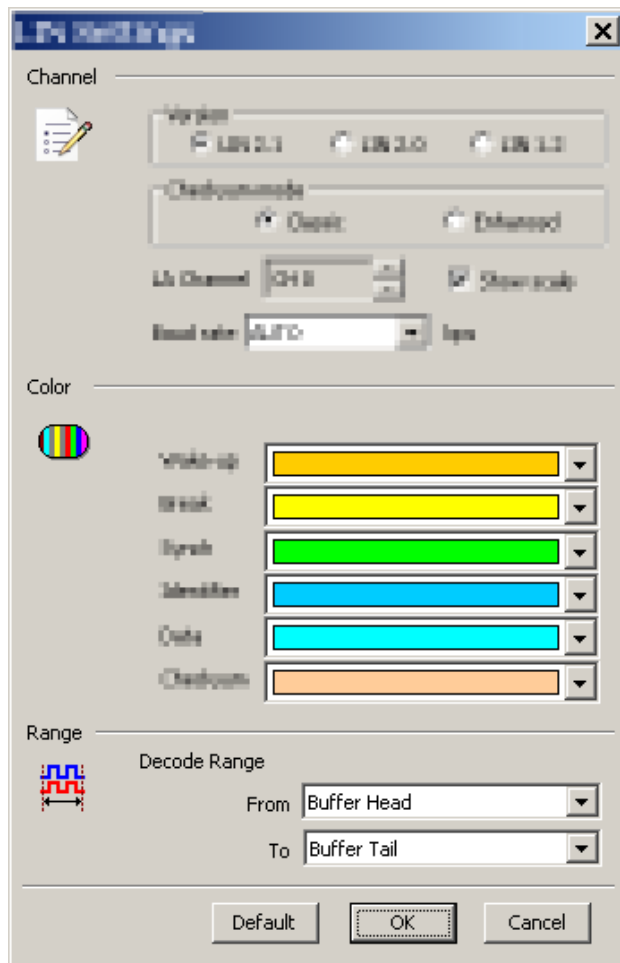
Method 2:

Click Add Bus Decode in the Label menu or right-click the label field to show the dialog box.

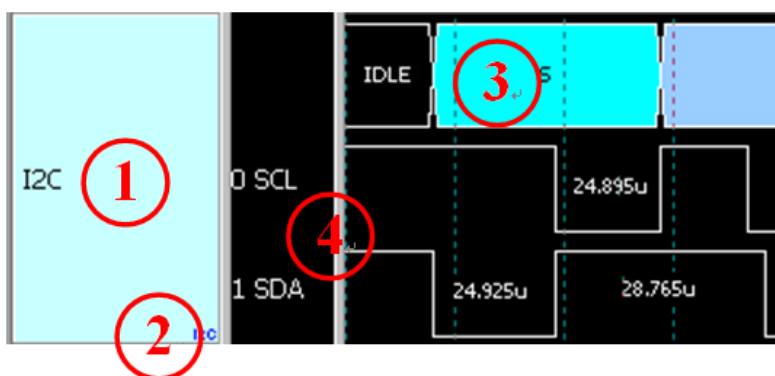
Advance channel setting



1. **Bus Name:** Enter the label name with 31 characters or less. (Chinese word expresses two characters.)
2. **Color:** Set the waveform color.
3. **Display the waveforms with decode**
4. **Display the waveforms with its decode together.**
5. **Advance:**



Set the decode parameters or press **OK** to use default settings. There are “Channel”, “Color”, “Range” settings



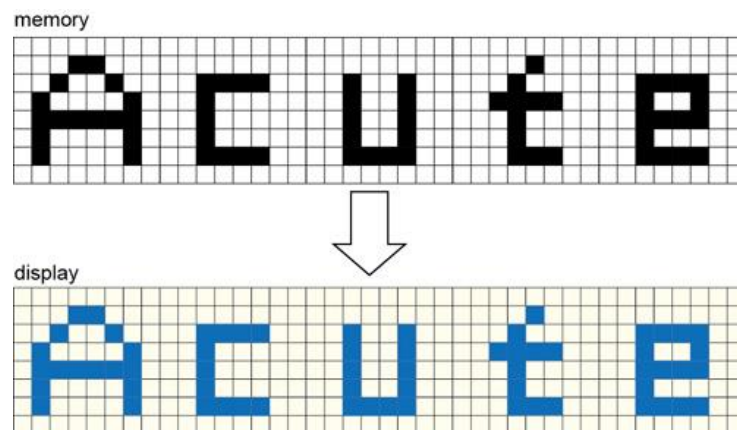
1. Bus name
2. Decode type
3. Result
4. Channel name & signal

Specially Bus Decode:

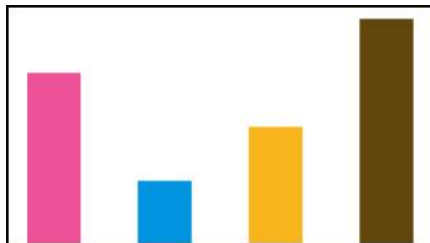
The bus decodes display the data in text format, but some decodes are able to show the original form for the data such as voice (I2S decode...), image, analog waveform (ADC decode) etc.

In the future, we will extend the original form display to more applications like:

LCD/CMOS image sensor bus decodes:



Statistic or Bar chart:



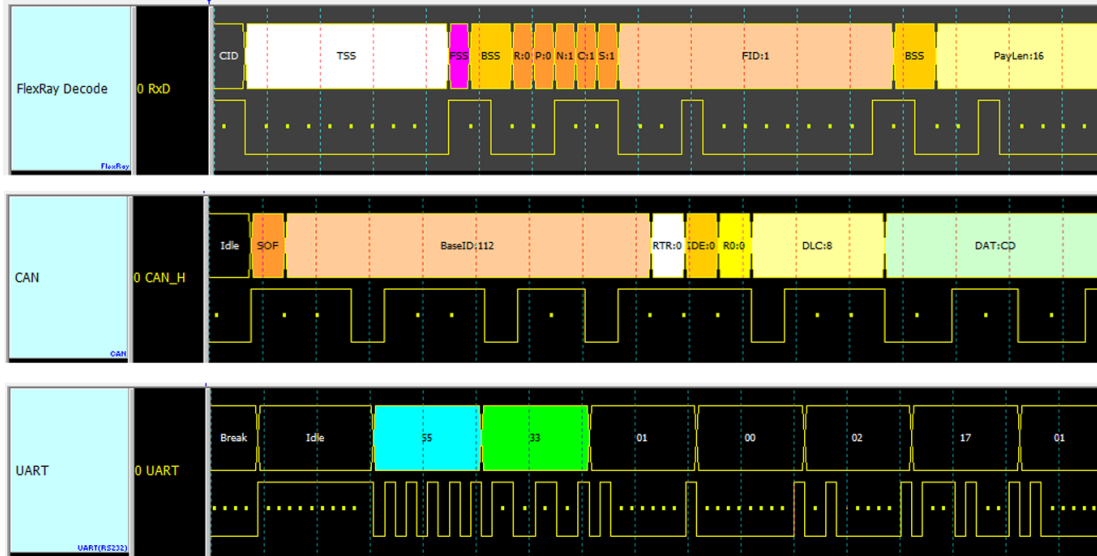
RPM:



The following original data form display for bus decodes are already available in the past.

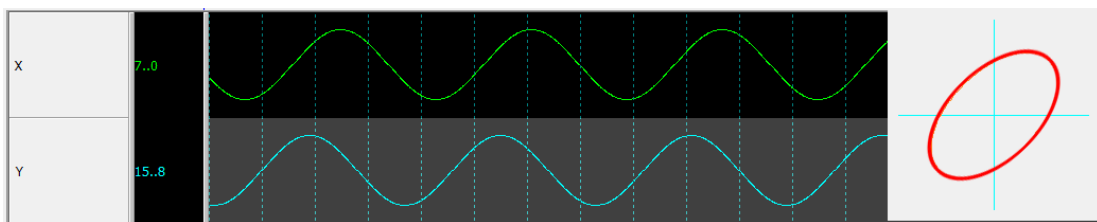
UART/CAN/FlexRay..bus decodes (released in 2009/9, LA Viewer Ver. 2.0):

The data is displayed according to bit points in order to calculate the bit number °



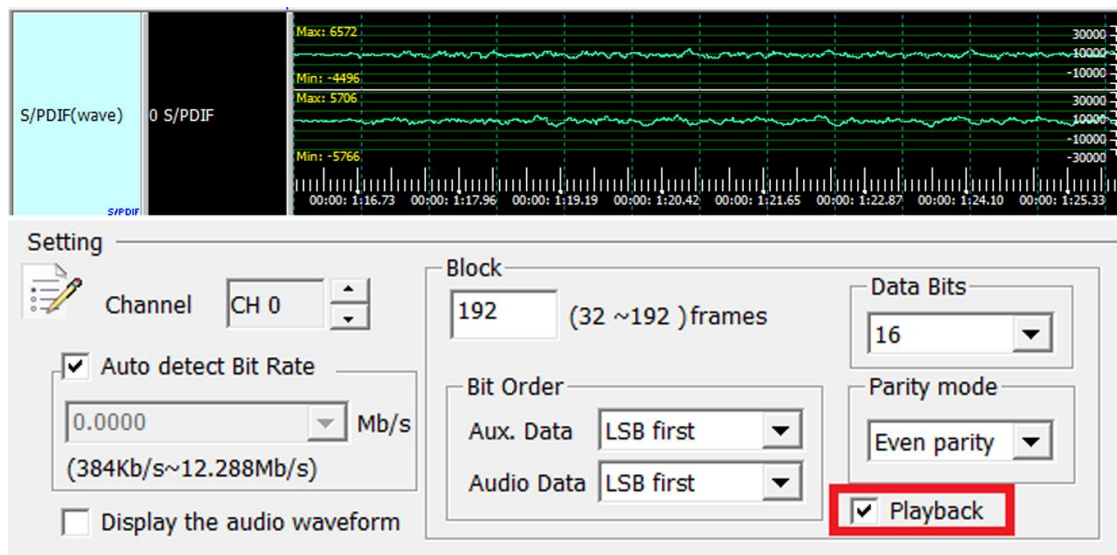
Lissajous analysis (released in 2009/09, LA Viewer Ver.2.0):

Display the signal in graph by X-Y or I-Q data. °



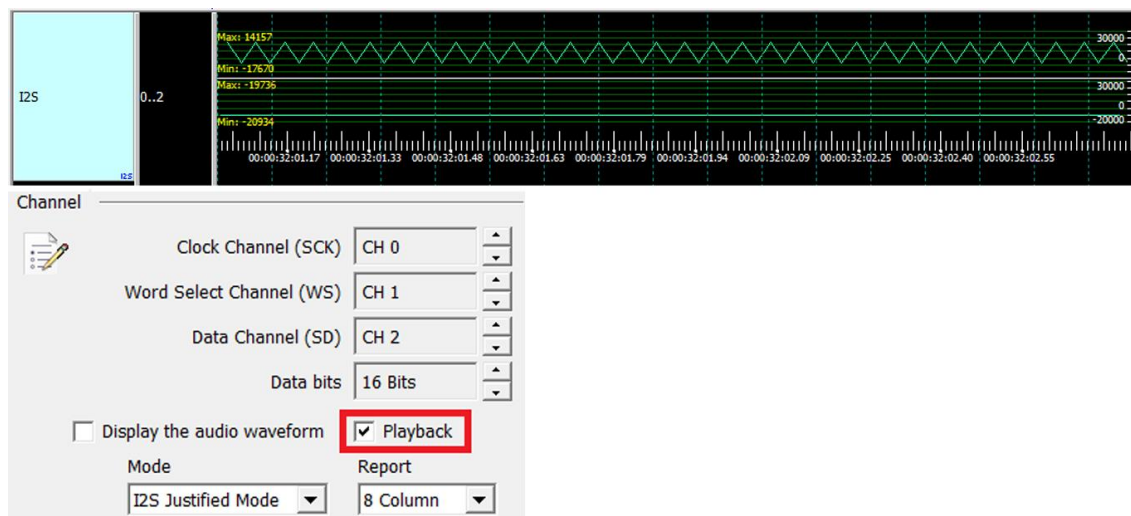
S/PDIF analysis (2010/11, LA Viewer Ver. 2.5):

Display the data in sound waveform °



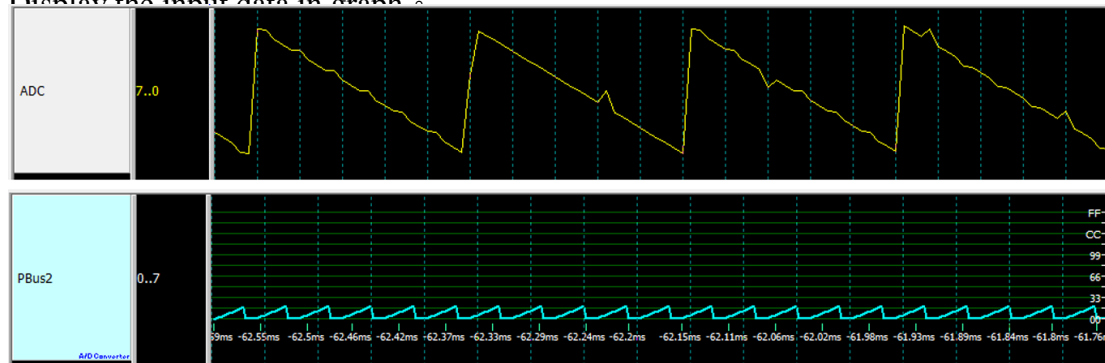
I2S analysis (2011/09, Ver. 2.6.3): 分析 (2011/09, LA Viewer Ver 2.6.3)

Display the data in sound waveform °



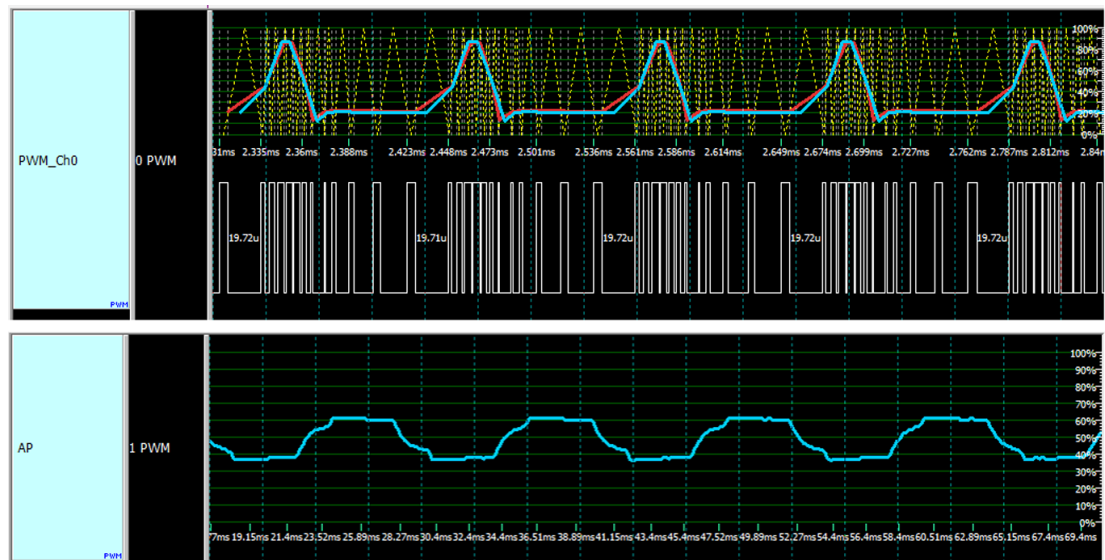
ADC bus decode (2012/08, LA Viewer Ver. 2.7.3):

Display the input data in graph °



PWM analysis (2012/08, LA Viewer Ver. 2.7.3):

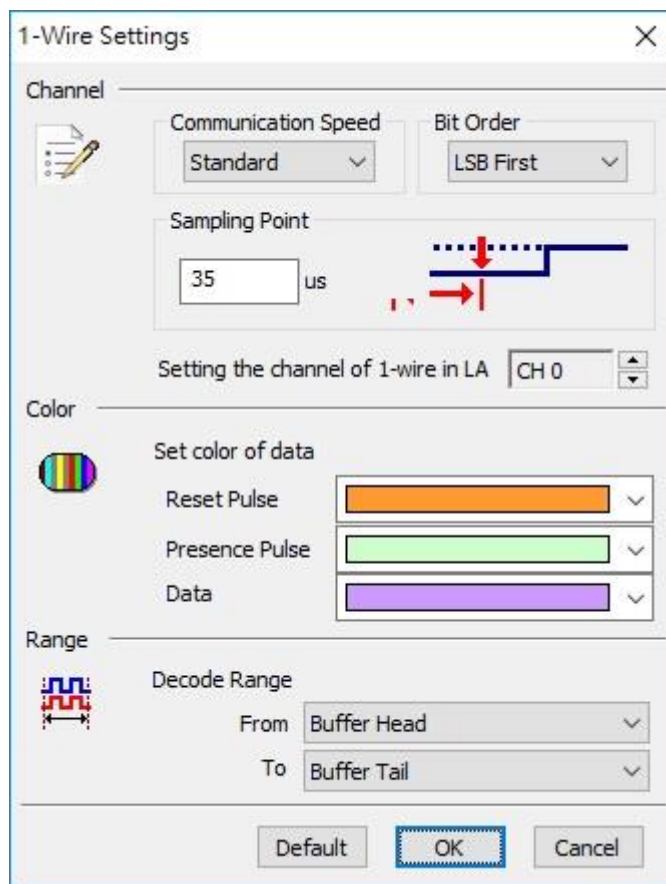
Restore and display the data in the waveform window as percentile or frequency °



1-Wire

The 1-Wire bus has data bits (Reset Pulse, Presence Pulse, Write 1, Write 0, Read 1, Read 0) in standard or overdrive speed as the diagram below.

Settings



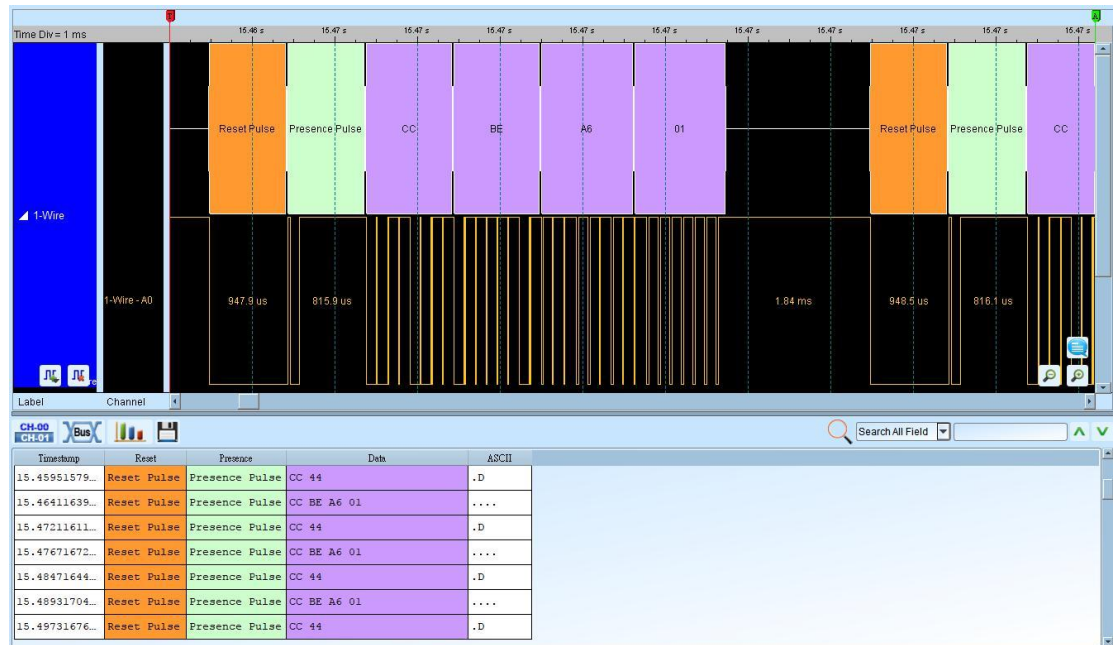
Communication Speed: Standard or overdrive.

Bit Order: LSB first or MSB first.

Sampling point: Set the sampling point N microseconds (us) after the beginning of each data bit.

Result

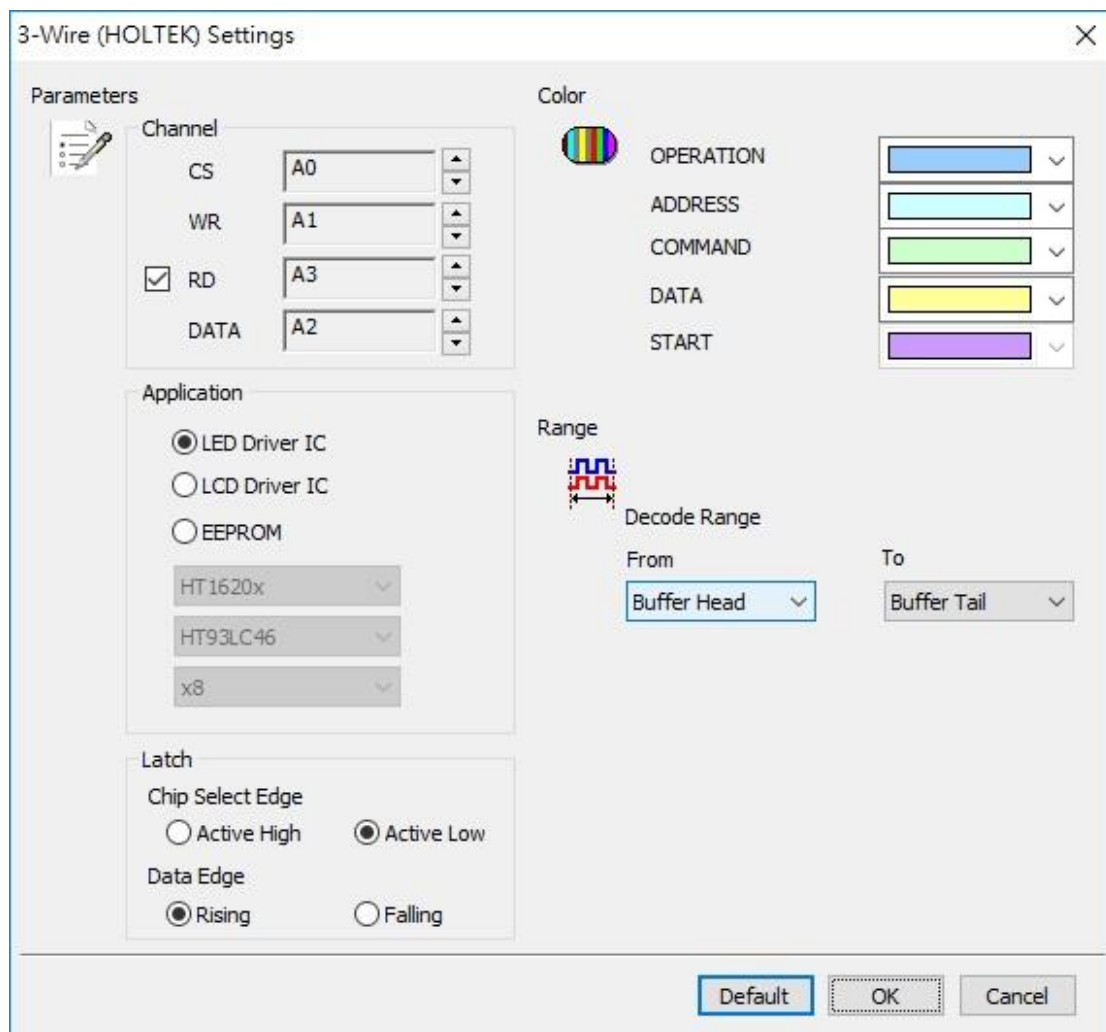
Click OK to run the 1-Wire decode and see the result on the Waveform Window below.



3-Wire

3-Wire protocol is established by HOLTEK SEMICONDUCTOR INC. It's Applied to control LED/LCD driver IC or EEPROM.

Settings



The image shows a software dialog box titled "3-Wire (HOLTEK) Settings". It is divided into several sections:

- Parameters:** Contains a list of channels with their assigned addresses: CS (A0), WR (A1), RD (checked, A3), and DATA (A2). Each address is in a text box with up/down arrow buttons.
- Application:** Features three radio buttons: "LED Driver IC" (selected), "LCD Driver IC", and "EEPROM". Below them are three dropdown menus: "HT1620x", "HT93LC46", and "x8".
- Latch:** Includes two groups of radio buttons. "Chip Select Edge" has "Active High" and "Active Low" (selected). "Data Edge" has "Rising" (selected) and "Falling".
- Color:** A vertical list of five color-coded boxes: OPERATION (blue), ADDRESS (cyan), COMMAND (green), DATA (yellow), and START (purple). Each box has a dropdown arrow.
- Range:** Includes a waveform icon and the text "Decode Range". Below it are two dropdown menus: "From" (set to "Buffer Head") and "To" (set to "Buffer Tail").

At the bottom right, there are three buttons: "Default", "OK", and "Cancel".

Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

LED Driver IC: Select LED driver IC application.

LCD Driver ID: Select LCD driver IC application.

EEPROM: Select EEPROM application.

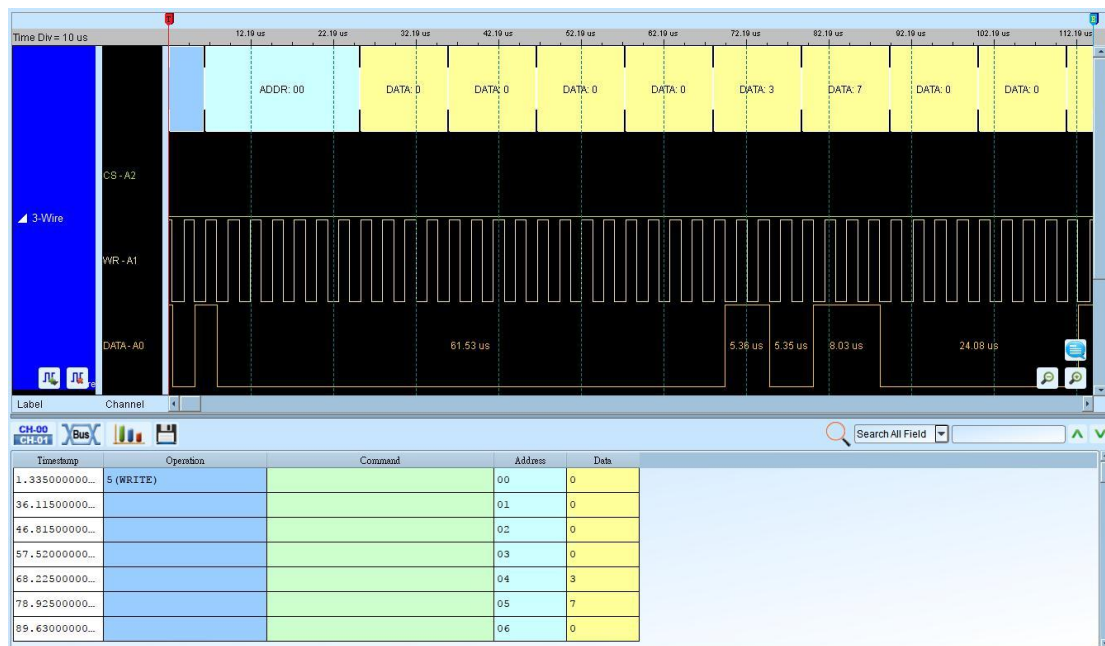
Active High: Select Active High.

Active Low: Select low chip select (CS).

Rising: Select Rising Data Edge.

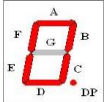
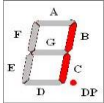
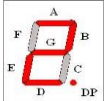
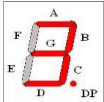
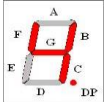
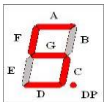
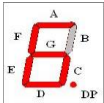
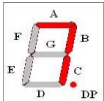
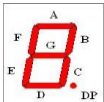
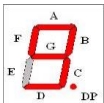
Falling: Select Falling Data Edge.

Result

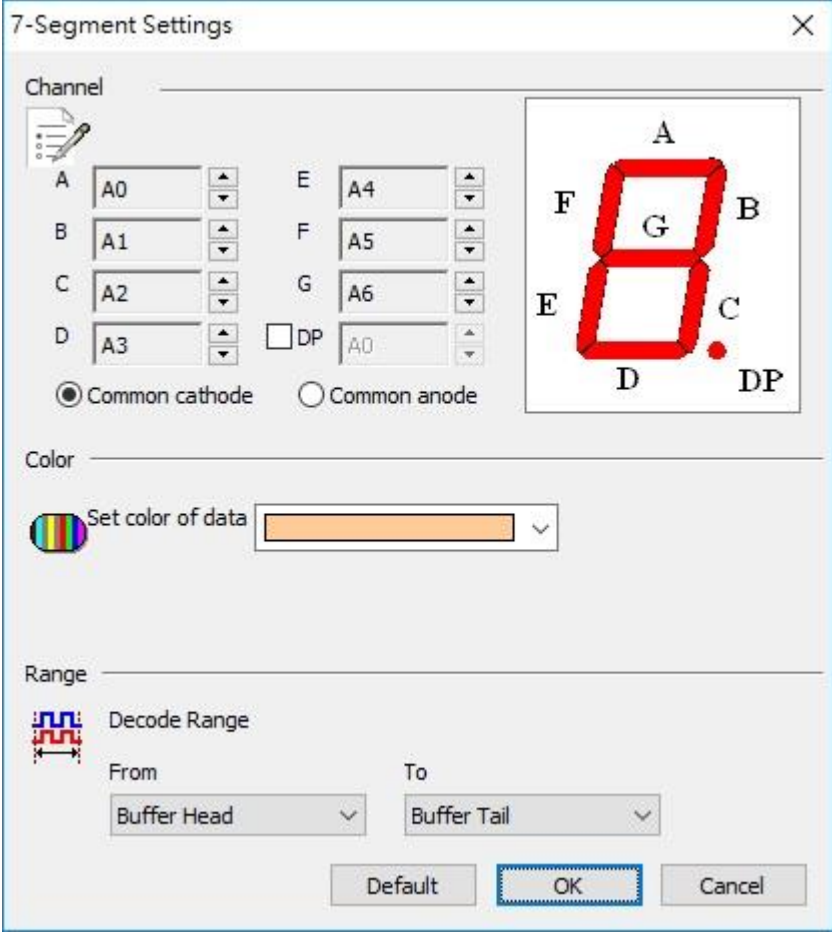


7-Segment

A seven-segment display, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.

Digit	LED	A	B	C	D	E	F	G
0		ON	ON	ON	ON	ON	ON	OFF
1		OFF	ON	ON	OFF	OFF	OFF	OFF
2		ON	ON	OFF	ON	ON	OFF	ON
3		ON	ON	ON	ON	OFF	OFF	ON
4		OFF	ON	ON	OFF	OFF	ON	ON
5		ON	OFF	ON	ON	OFF	ON	ON
6		ON	OFF	ON	ON	ON	ON	ON
7		ON	ON	ON	OFF	OFF	OFF	OFF
8		ON	ON	ON	ON	ON	ON	ON
9		ON	ON	ON	ON	OFF	ON	ON

Settings



The dialog box is titled "7-Segment Settings" and contains the following sections:

- Channel:** Includes a list icon and a grid of segment assignment controls. Segments A, B, C, and D are assigned to A0, A1, A2, and A3 respectively. Segments E, F, and G are assigned to A4, A5, and A6 respectively. There is an unchecked checkbox for "DP" assigned to A0. Below the grid are radio buttons for "Common cathode" (selected) and "Common anode".
- Color:** Features a color selection icon and a text field labeled "Set color of data" with a dropdown arrow, currently showing an orange color.
- Range:** Includes a waveform icon and a "Decode Range" section with "From" and "To" dropdown menus, both set to "Buffer Head" and "Buffer Tail" respectively.

At the bottom right, there are three buttons: "Default", "OK" (highlighted with a blue border), and "Cancel".

On the right side of the dialog, there is a diagram of a 7-segment display. The segments are labeled A (top), B (top-right), C (bottom-right), D (bottom), E (bottom-left), F (top-left), and G (middle). A decimal point (DP) is shown at the bottom right. The display is currently showing the digit '8' in red.

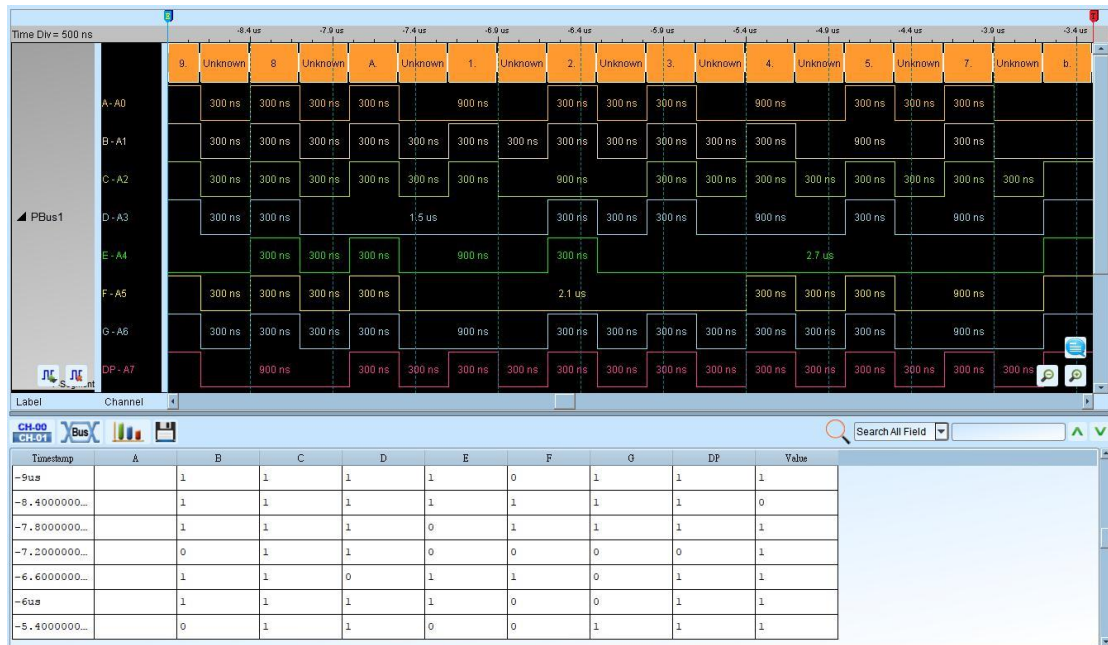
Channel: Show the selected channel (CH 0).

DP: to analysis decimal point.

Common cathode/anode: Show the same cathode or anode.

Result

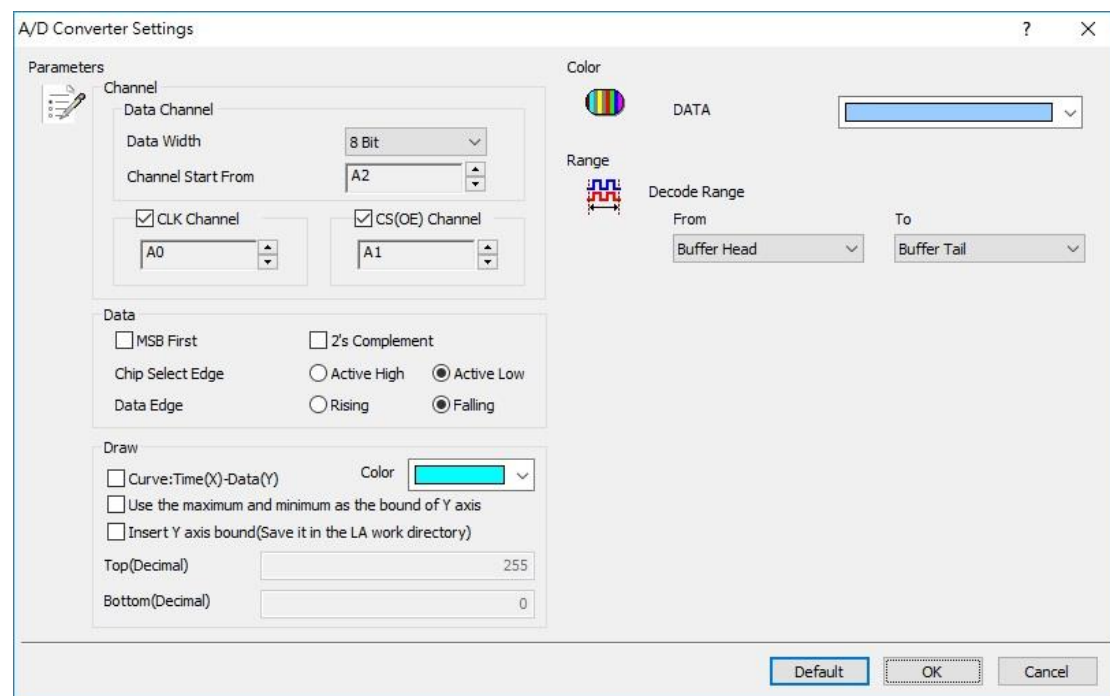
Click **OK** to run the 7 Segment decode and see the result on the Waveform Window below.



A/D Converter

A/D Converter (Analog-To-Digital Converter), is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form.

Settings



Data Channel Start From: ADC data channel start from

CLK Channel: ADC clock in channel

CS(OE) Channel: ADC chip select (output enable) channel

Data Width: ADC data width, range: 4Bit ~ 32Bit

MSB First: Data bit starts form MSB; LSB defaulted

2's Complement: Show the 2's complement result.

Chip Select Edge: Set the chip select edge; Active Low defaulted

Data Edge: Set the Data Edge; Falling Edge defaulted

Curve: Time(X)-Data(Y) Show the diagram in form of time as X axis; data as Y axis.

Color: Select the curve color

Use the maximum and minimum as the bound of Y axis: Use the maximum data as the top bound of Y axis and minimum data as the bottom bound of Y axis.

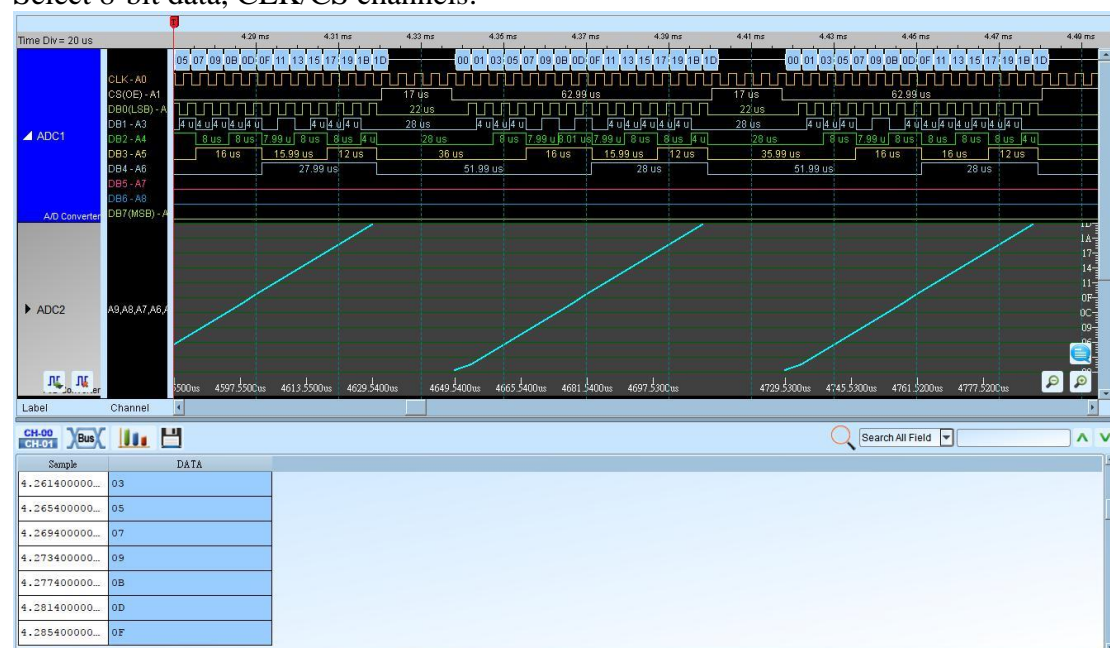
Insert Y axis bound: Set the maximum and minimum bounds of Y axis.

Note: When Insert Y axis boundaries is activated (Save it in the LA file directory), the Top and Bottom values will always be saved as an independent text file named as ADC.txt, different from the waveform file, at file work directory unless a different name is assigned. If you need the specific boundary settings, please save it, so you can reload the settings next time.

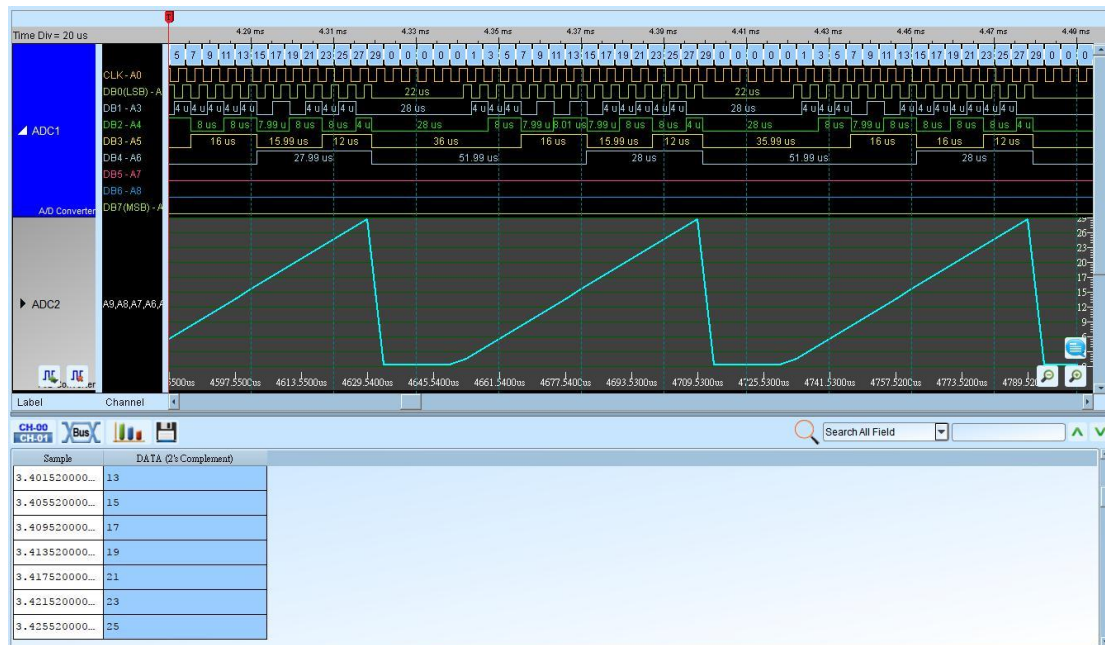
Result

Click **OK** to run the A/D Converter decode and see the result on the Waveform Window below.

Select 8-bit data, CLK/CS channels:



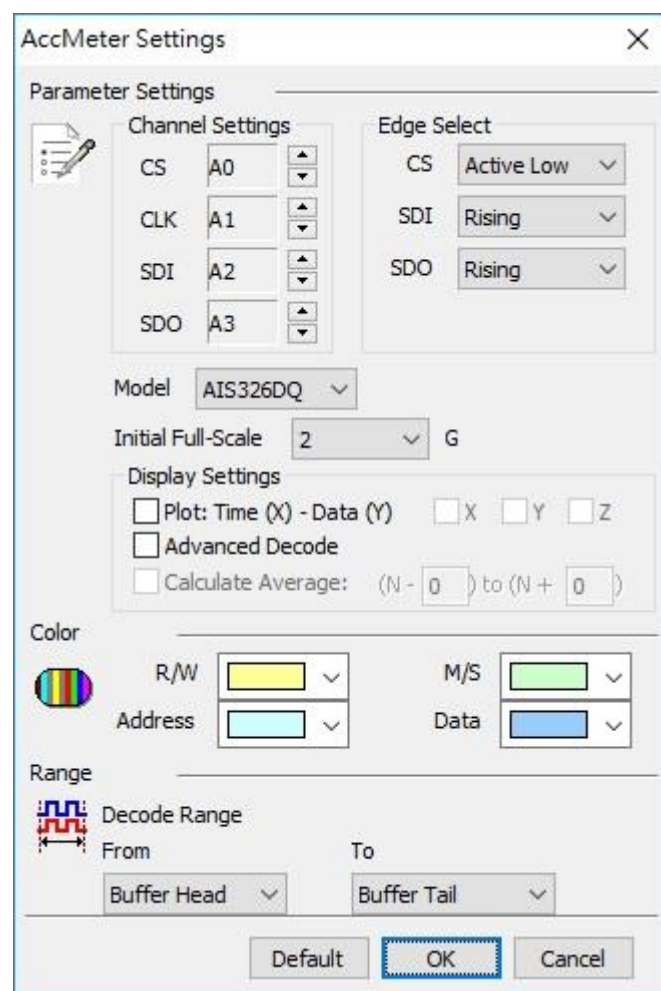
Select 8-bit data:



AcceleroMeter

AcceleroMeter (AccMeter) decoder is the SPI interfaced accelerometer data decoder, which provides bus value to acceleration value conversion and curve drawing function.

Settings



The image shows the 'AccMeter Settings' dialog box. It is divided into several sections: 'Parameter Settings' (containing 'Channel Settings' and 'Edge Select'), 'Model' (a dropdown menu), 'Initial Full-Scale' (a dropdown menu), 'Display Settings' (checkboxes for 'Plot: Time (X) - Data (Y)', 'Advanced Decode', and 'Calculate Average'), 'Color' (color pickers for 'R/W', 'Address', 'M/S', and 'Data'), and 'Range' (a section with a waveform icon and 'Decode Range' sub-section containing 'From' and 'To' dropdowns). At the bottom are 'Default', 'OK', and 'Cancel' buttons.

Section	Parameter	Value
Channel Settings	CS	A0
	CLK	A1
	SDI	A2
	SDO	A3
Edge Select	CS	Active Low
	SDI	Rising
	SDO	Rising
Model	AIS326DQ	
Initial Full-Scale	2 G	
Display Settings	Plot: Time (X) - Data (Y)	<input type="checkbox"/> X <input type="checkbox"/> Y <input type="checkbox"/> Z
	Advanced Decode	<input type="checkbox"/>
	Calculate Average	(N - 0) to (N + 0)
Color	R/W	Yellow
	Address	Cyan
Color	M/S	Green
	Data	Blue
Range	From	Buffer Head
	To	Buffer Tail

CS: Chip Select, must specified the active state of the CS pin.

CLK: Clock

SDI: Data Input Pin, must specified the data sampling edge.

SDO: Data Output Pin, must specified the data sampling edge.

Model: The IC model of the target accelerometer.

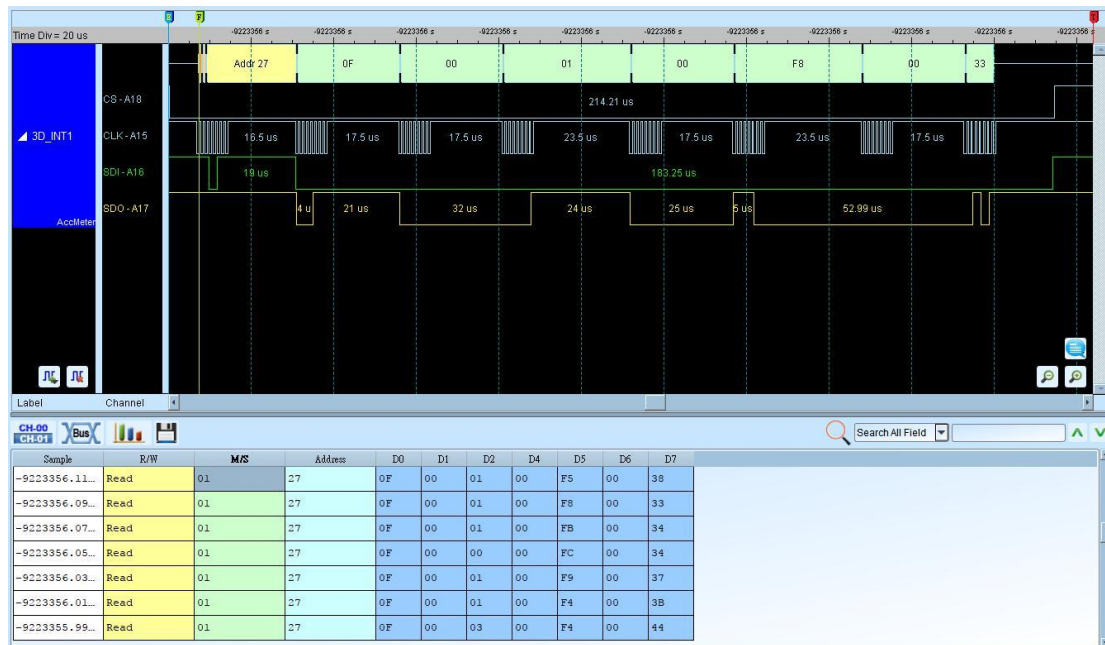
Initial Full-Scale: The default Full-Scale setting.

Plot: Enable/Disable to display the waveform in Time-Value curve.

Advanced Decode: Enable/Disable the address, value convert function.

Result

Standard decoder result



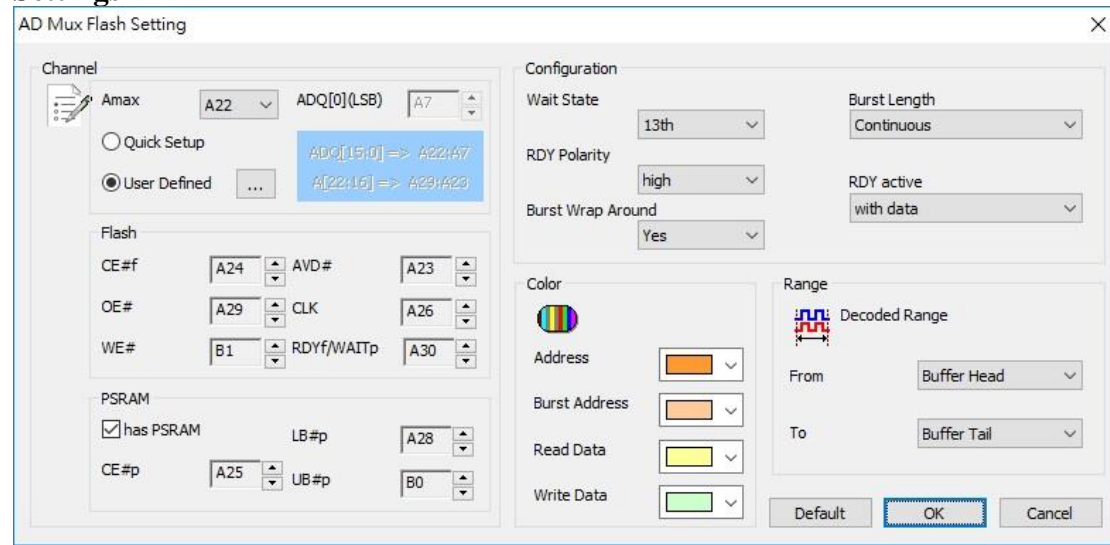
Advanced decode result + Time-Value curve display



AD-Mux Flash

AD-Mux Flash is one kind of parallel flash that utilize an Address and Data multiplexed interface.

Settings



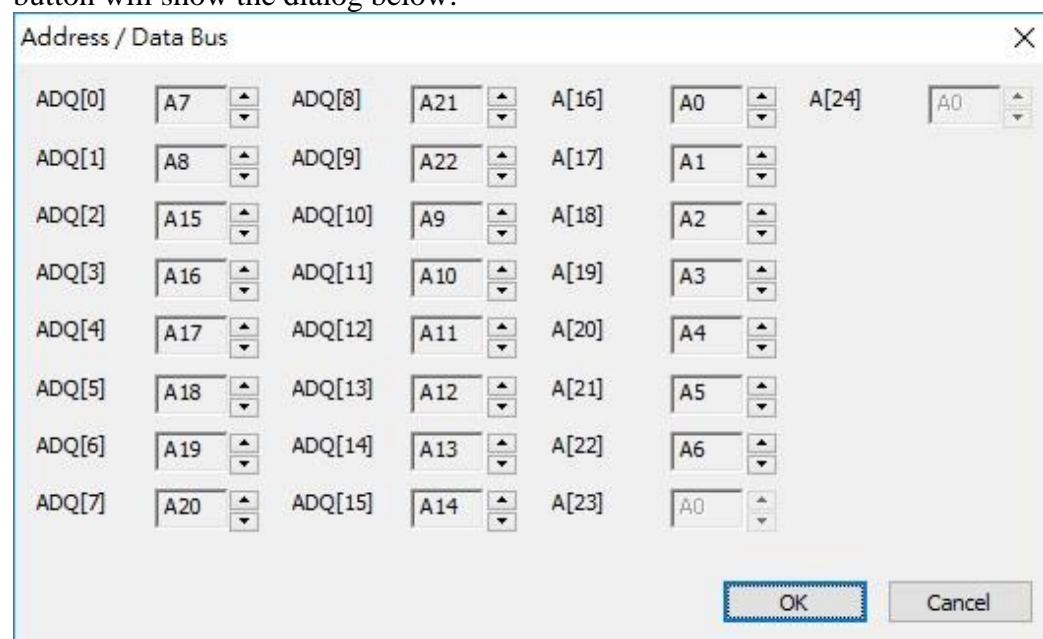
The AD Mux Flash Setting dialog box is divided into several sections:

- Channel:** Includes a list of channels (Amax, ADQ[0](LSB), etc.) and a selection for Quick Setup or User Defined. A blue box highlights the mapping: ADQ[15:0] => A22:A7 and A[22:15] => A23:A23.
- Flash:** Contains settings for CE#f (A24), AVD# (A23), OE# (A29), CLK (A26), WE# (B1), RDYf/WAITp (A30), and PSRAM options (has PSRAM, LB#p (A28), CE#p (A25), UB#p (B0)).
- Configuration:** Includes Wait State (13th), Burst Length (Continuous), RDY Polarity (high), RDY active (with data), and Burst Wrap Around (Yes).
- Color:** A color selection tool for Address, Burst Address, Read Data, and Write Data.
- Range:** A range selection tool for Decoded Range, From (Buffer Head), and To (Buffer Tail).

Buttons at the bottom include Default, OK, and Cancel.

Amax: Setting the number of address pin.

Quick Setup/User Defined: Only set ADQ[0](LSB) when select the Quick Setup, other channels will be set automatically. When check User Defined and press the button will show the dialog below:



The Address / Data Bus dialog box displays a grid of address and data bus settings:

ADQ[0]	A7	ADQ[8]	A21	A[16]	A0	A[24]	A0
ADQ[1]	A8	ADQ[9]	A22	A[17]	A1		
ADQ[2]	A15	ADQ[10]	A9	A[18]	A2		
ADQ[3]	A16	ADQ[11]	A10	A[19]	A3		
ADQ[4]	A17	ADQ[12]	A11	A[20]	A4		
ADQ[5]	A18	ADQ[13]	A12	A[21]	A5		
ADQ[6]	A19	ADQ[14]	A13	A[22]	A6		
ADQ[7]	A20	ADQ[15]	A14	A[23]	A0		

Buttons at the bottom include OK and Cancel.

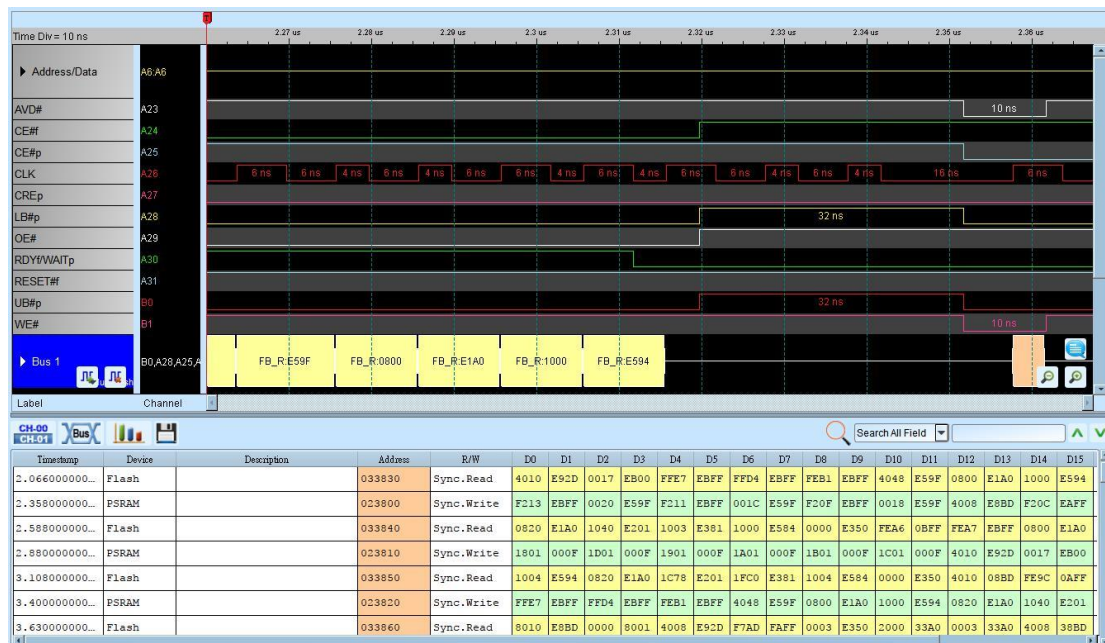
Flash: Control pins of flash.

PSRAM: Control pins of PSRAM. Some MCP include Flash and PSRAM in one package. It will decode PSRAM at the same time when “has PSRAM” is checked.

Configuration: The default setting of configuration register. User must set here to make a correct analysis.

Result

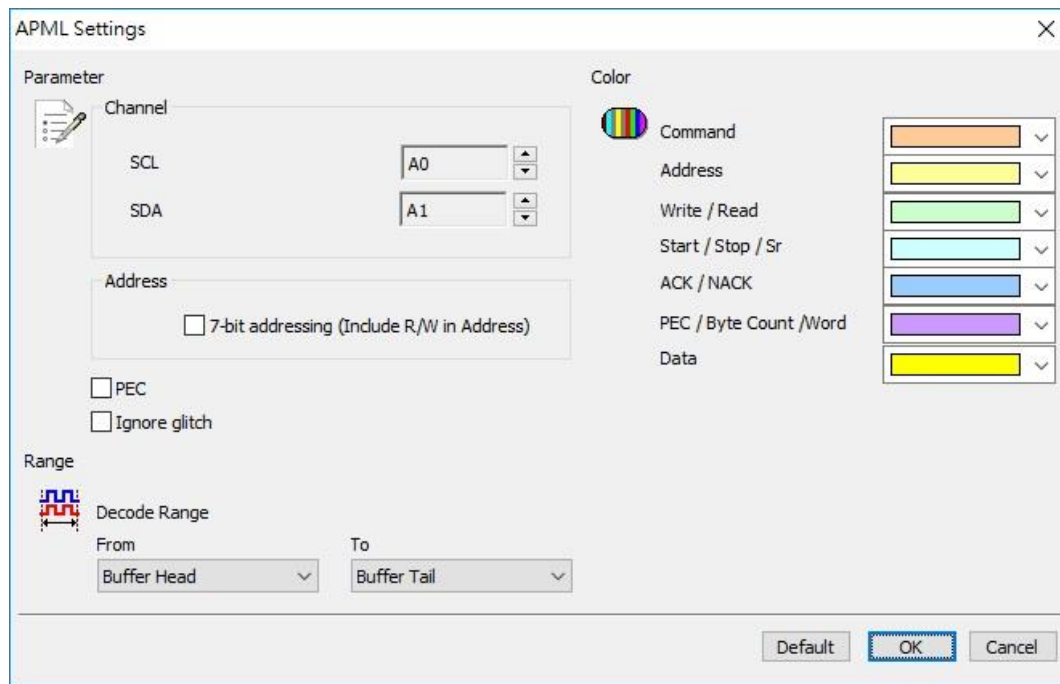
Click OK to run the AD-Mux Flash Decode and see result on the Waveform Windows below.



Advanced Platform Management Link (APML)

APML protocol is established by AMD for it's Opteron CPU platform.

Settings



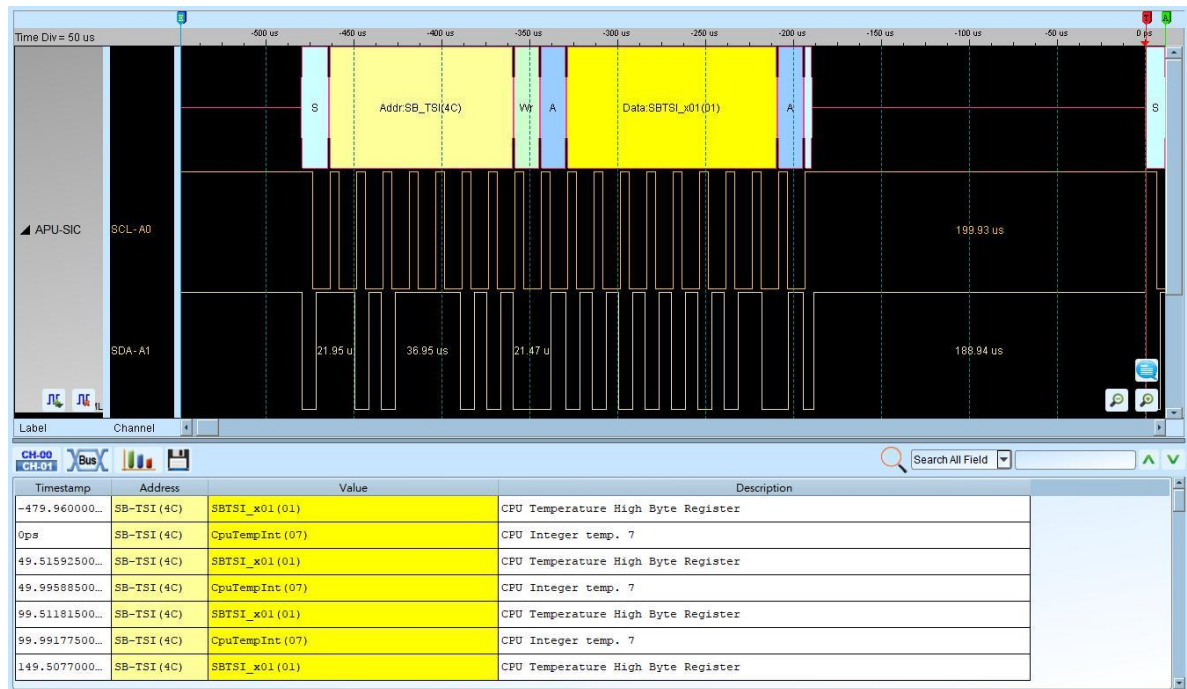
Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

PEC: Packet Error Check.

Ignore glitch: Ignore the glitch when the slow transitions.

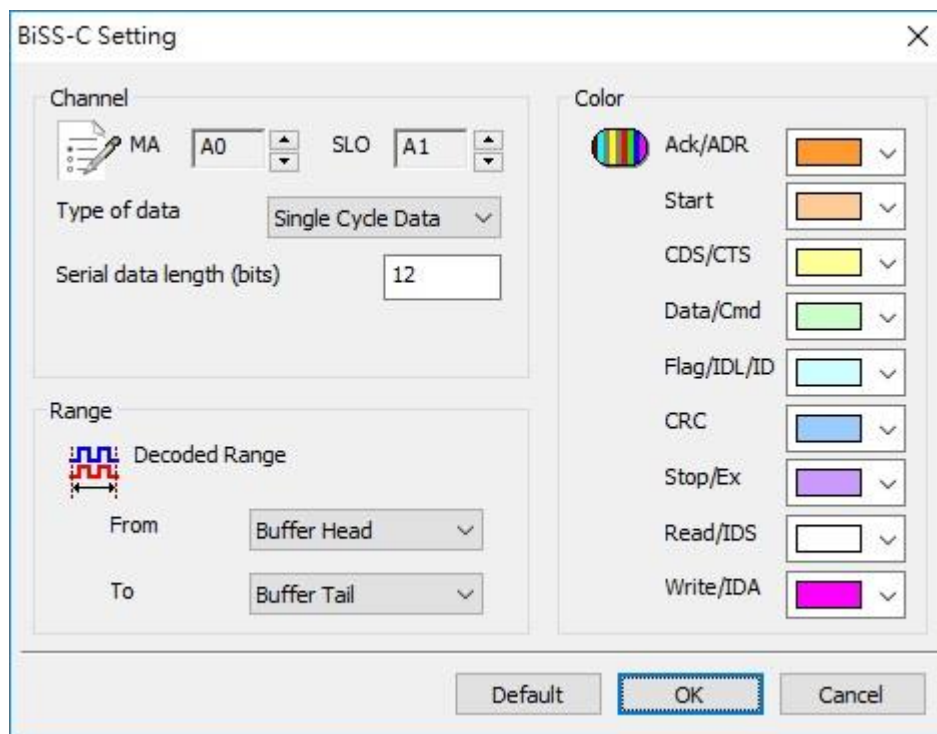
Result



BiSS-C

BiSS-C (Bidirectional Synchronous Serial C-mode) designed by Ic-Haus. The BiSS Interface is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort.

Settings



The BiSS-C Setting dialog box is divided into several sections. The 'Channel' section on the left includes a 'MA' dropdown set to 'A0' and an 'SLO' dropdown set to 'A1'. Below this, the 'Type of data' is set to 'Single Cycle Data' in a dropdown menu, and the 'Serial data length (bits)' is set to '12' in a text box. The 'Range' section below that features a 'Decoded Range' icon and two dropdowns: 'From' set to 'Buffer Head' and 'To' set to 'Buffer Tail'. On the right, the 'Color' section lists nine data fields with corresponding color selection boxes: Ack/ADR (orange), Start (light orange), CDS/CTS (yellow), Data/Cmd (light green), Flag/IDL/ID (cyan), CRC (blue), Stop/Ex (purple), Read/IDS (white), and Write/IDA (magenta). At the bottom, there are three buttons: 'Default', 'OK' (highlighted with a blue border), and 'Cancel'.

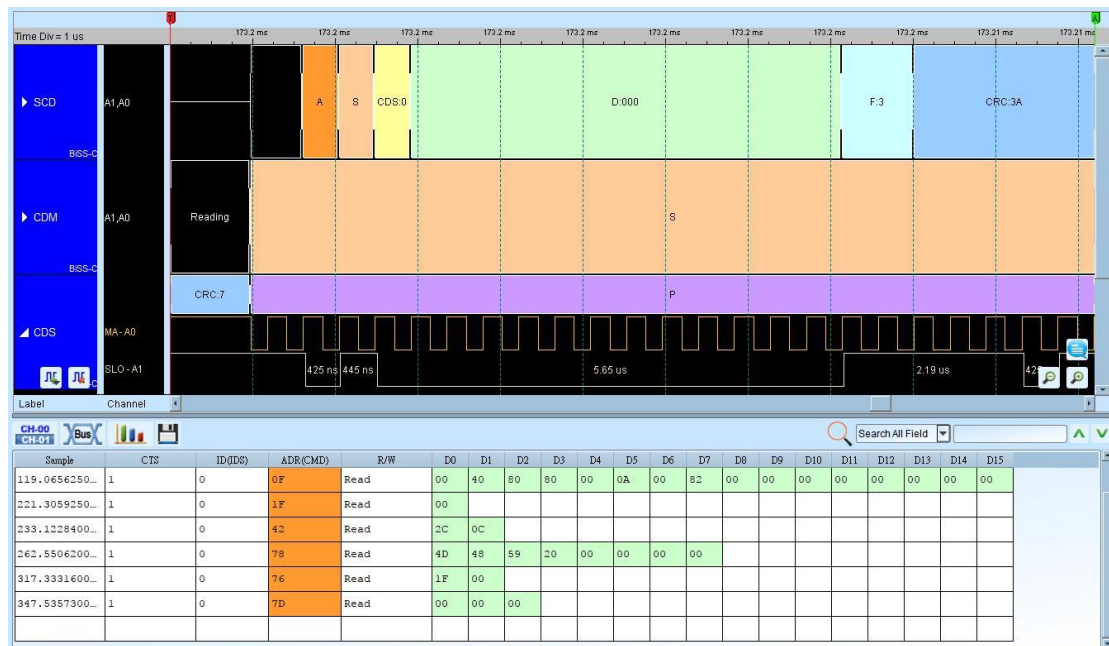
MA/SLO: Setting the channel of MA and SLO.

Type of data: Setting the type you want to decode. It include “Register Data-CDM”, “Register Data-CDS”, “Single Cycle Data”.

Serial data length(bits): Setting the data length when Single Cycle Data mode.

Result

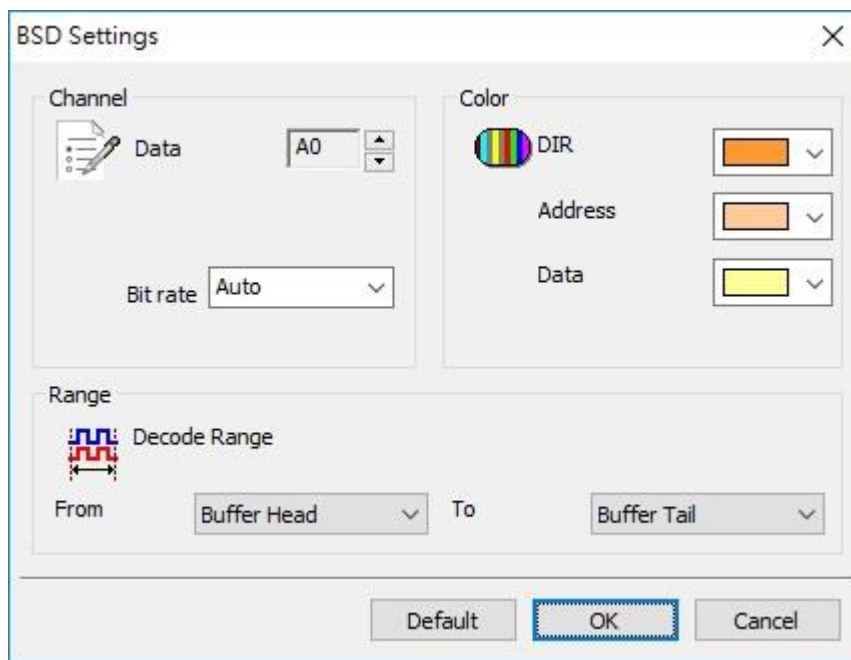
Click OK to run the BiSS-C Decode and see result on the Waveform Windows below.



BSD

BSD(Bit Serial Device) is a serial communications protocol for battery monitoring in automotive application.

Settings

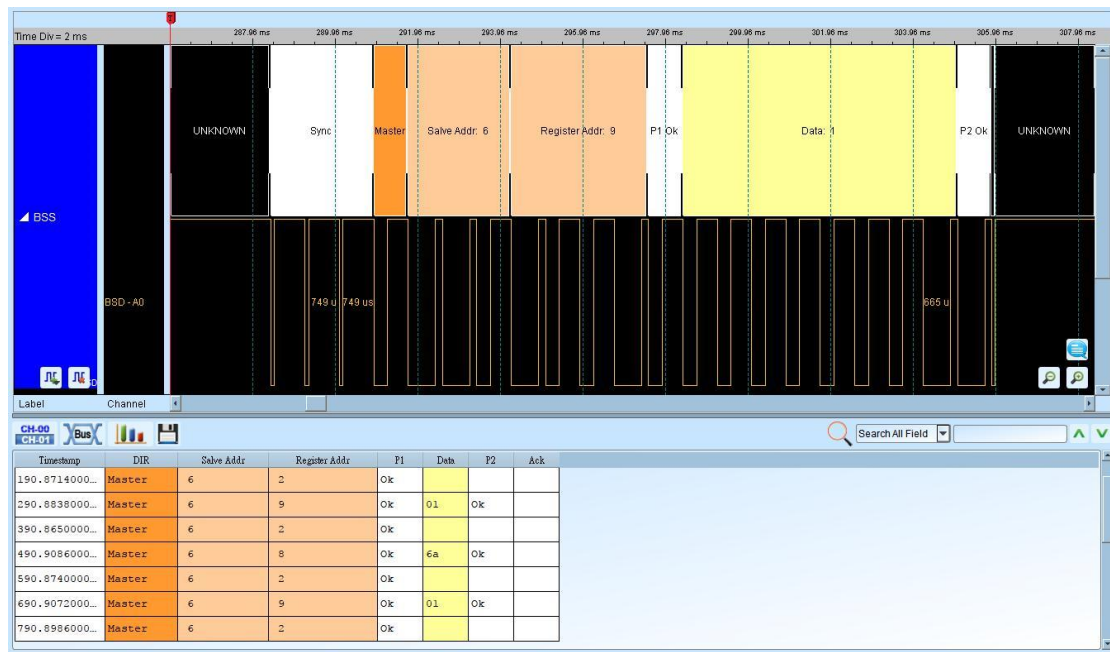


Data: The BSD data.

Bit rate: The bit rate of the BSD data

Result

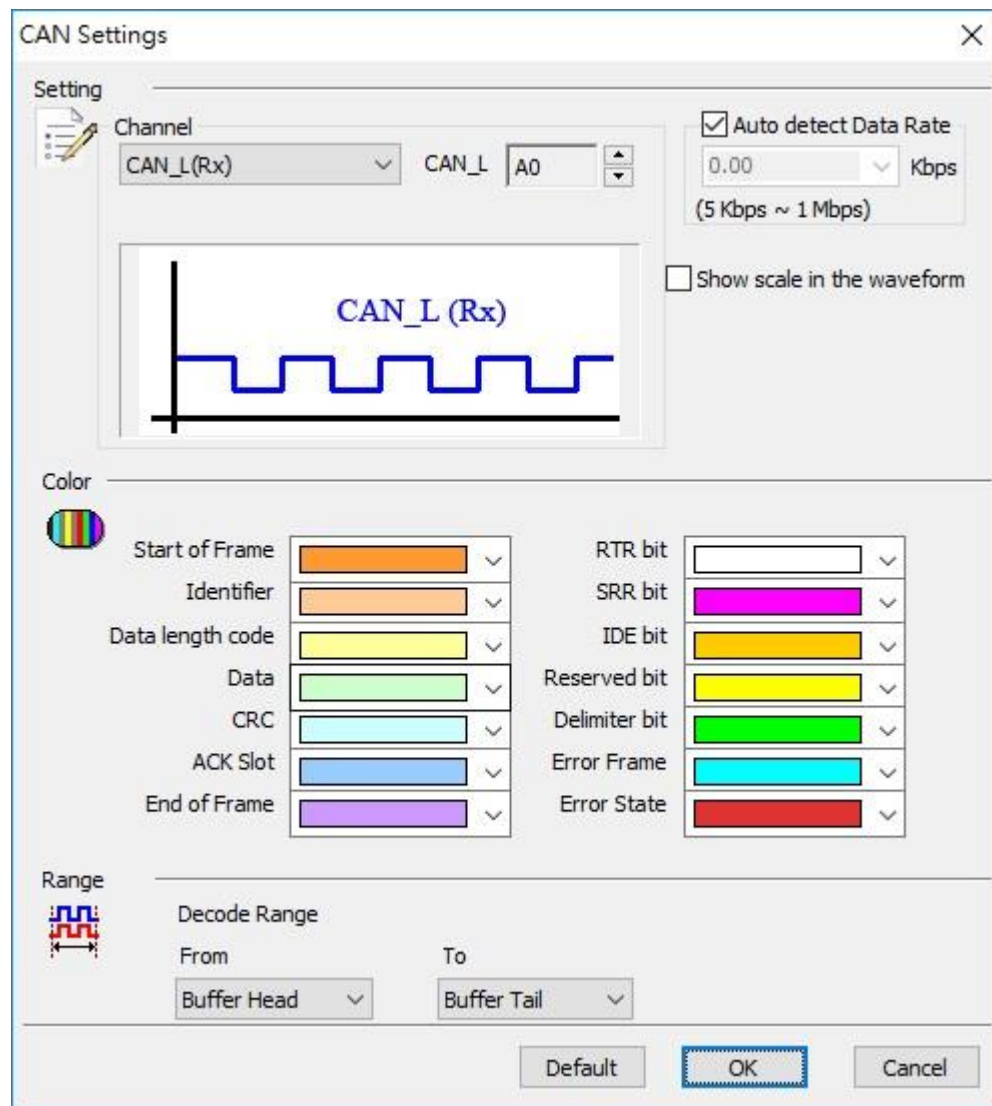
Click OK to run the BSD Decode and see result on the Waveform Windows below.



CAN

The Controller Area Network (CAN) protocol has version 2.0A (Basic CAN, 11 bits) and version 2.0B (Extended CAN or Peli CAN, 29 bits); both versions have four message types: Data Frame, Remote Frame, Error Frame and Overload Frame as the diagrams below. The CAN Bus has two kinds of data output: CAN High (CAN_H) and CAN Low (CAN_L).

Settings



Channel: The differential data from the DSO channel (CAN_H or CAN_L) is shown by default.

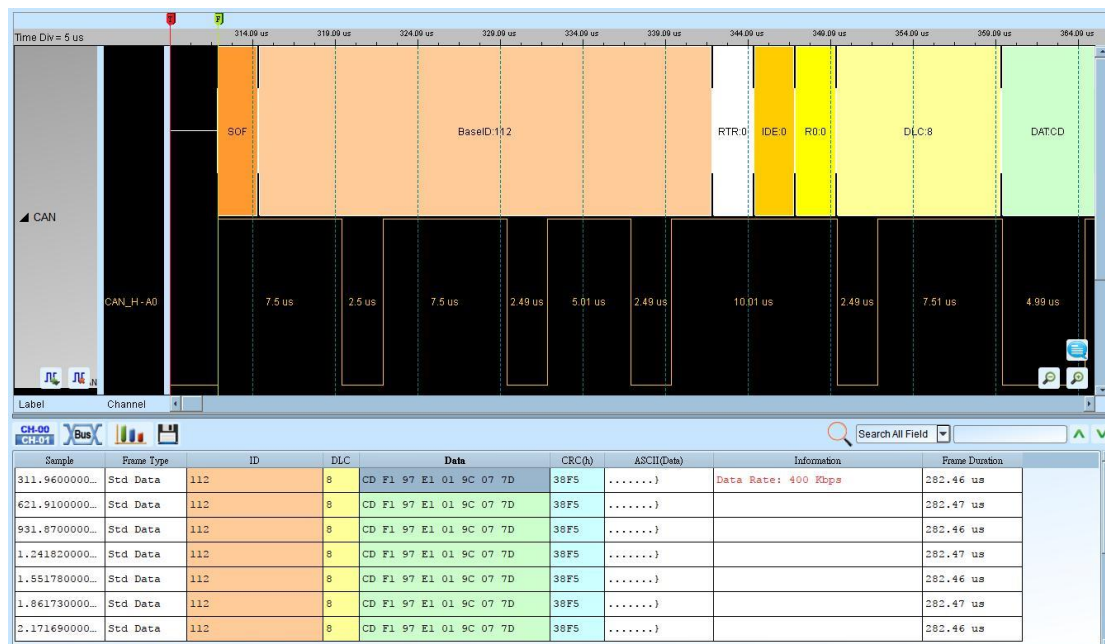
Auto detect Data Rate: Click to detect the CAN bit rate by the LA Viewer.

Show scale in the waveform: Display the scale in the Waveform Window.

Show scale in the waveform : Display the waveforms with scales.

Result

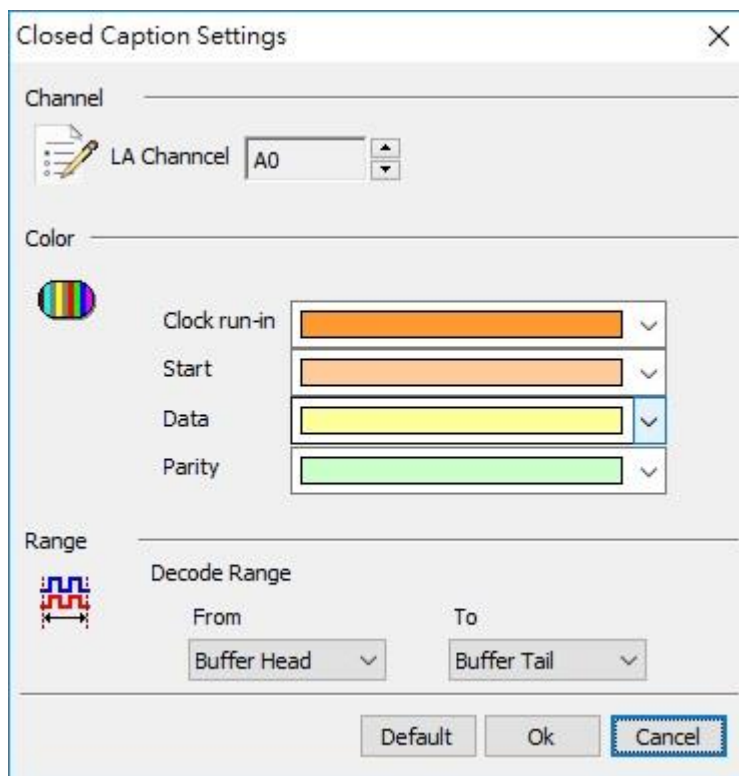
Click **OK** to run the CAN decode and see the result on the Waveform Window below.



Closed Caption

Closed captioning is the process of displaying text on a TV or video screen. The text is encoded in the video data stream.

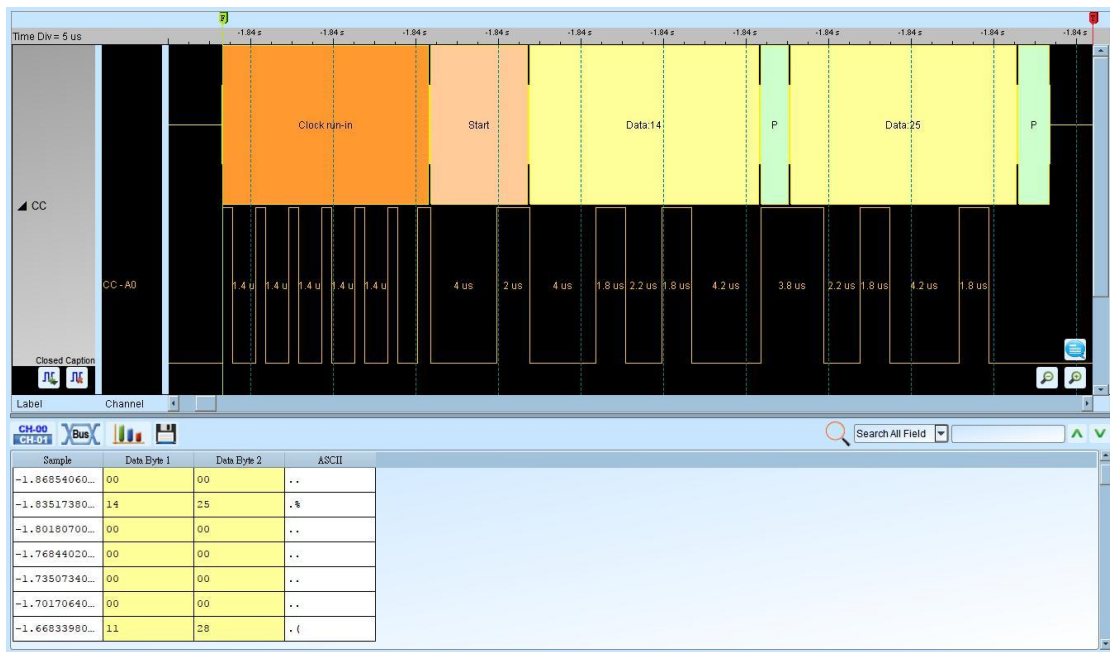
Settings



LA Channel: Show the selected channel (CH0).

Result

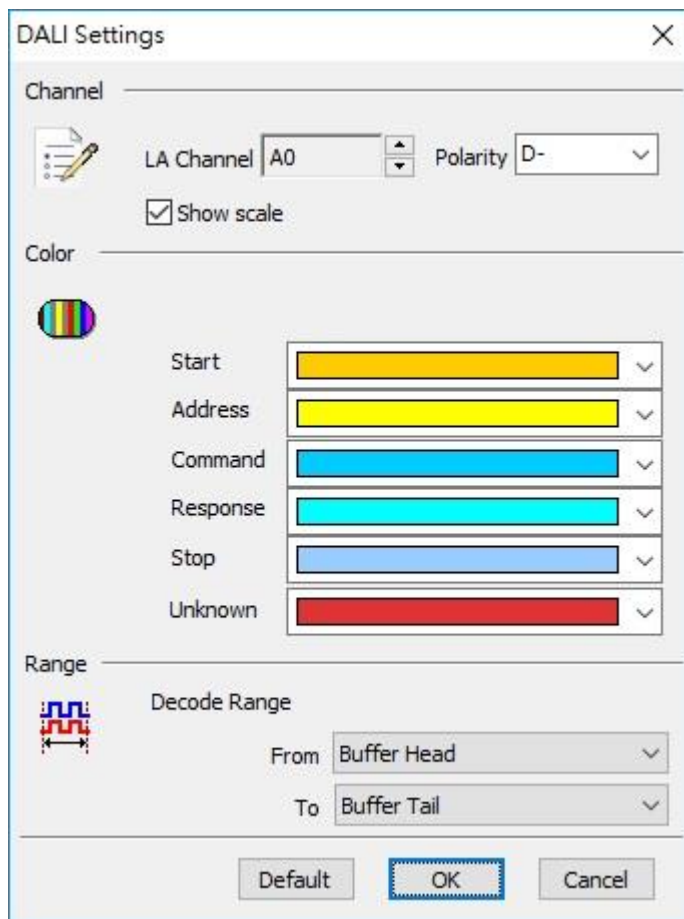
Click OK to run the Closed Caption Decode and see result on the Waveform Window below.



DALI

Digital Addressable Lighting Interface (DALI) is a technical standard for network-based systems that control lighting in buildings. The DALI standard, which is specified in the IEC 60929 standard for fluorescent lamp ballasts, encompasses the communications protocol and electrical interface for lighting control networks.

Settings



The DALI Settings dialog box is divided into three main sections: Channel, Color, and Range. The Channel section includes a 'LA Channel' dropdown menu set to 'A0', a 'Polarity' dropdown menu set to 'D-', and a checked 'Show scale' checkbox. The Color section features a color wheel icon and six color-coded bars for 'Start' (yellow), 'Address' (light yellow), 'Command' (cyan), 'Response' (light blue), 'Stop' (medium blue), and 'Unknown' (red). The Range section includes a 'Decode Range' section with 'From' and 'To' dropdown menus, both set to 'Buffer Head' and 'Buffer Tail' respectively. At the bottom are 'Default', 'OK', and 'Cancel' buttons.

LA Channel: Show the selected channel (CH0).

Polarity:

D-: Access side of the signal polarity is D-.

D+: Access side of the signal polarity is D+.

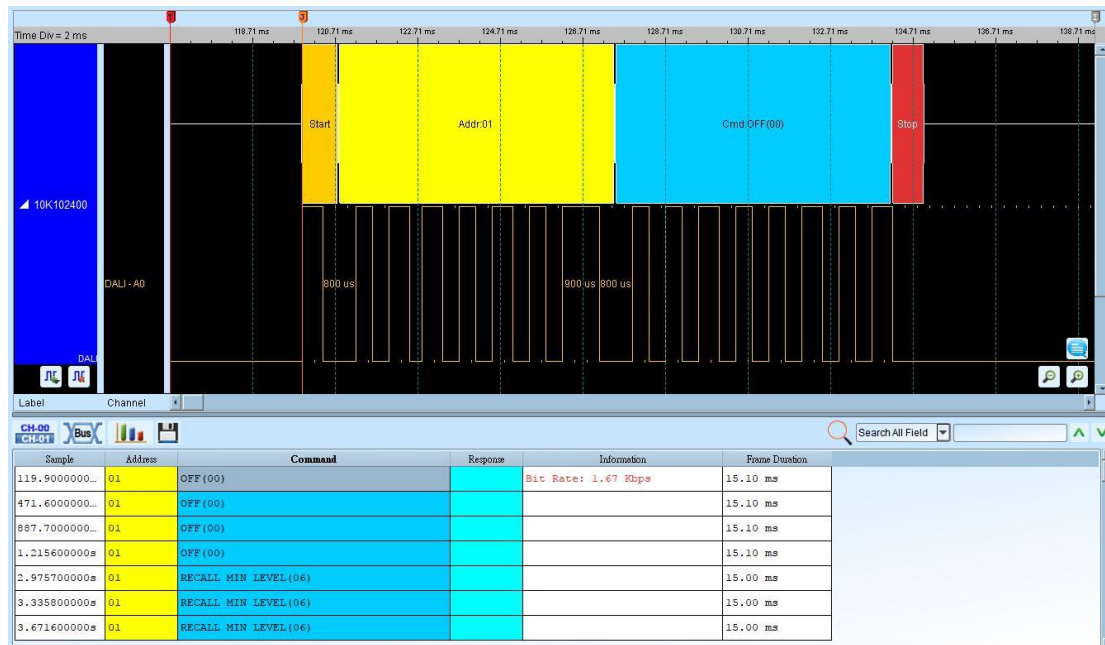
Auto: Automatically detect the polarity of the access end signal.

Show scale: Show Scale on the waveform.

Result

Click OK to run DALI Decode and see result on the Waveform Window below.

Send data



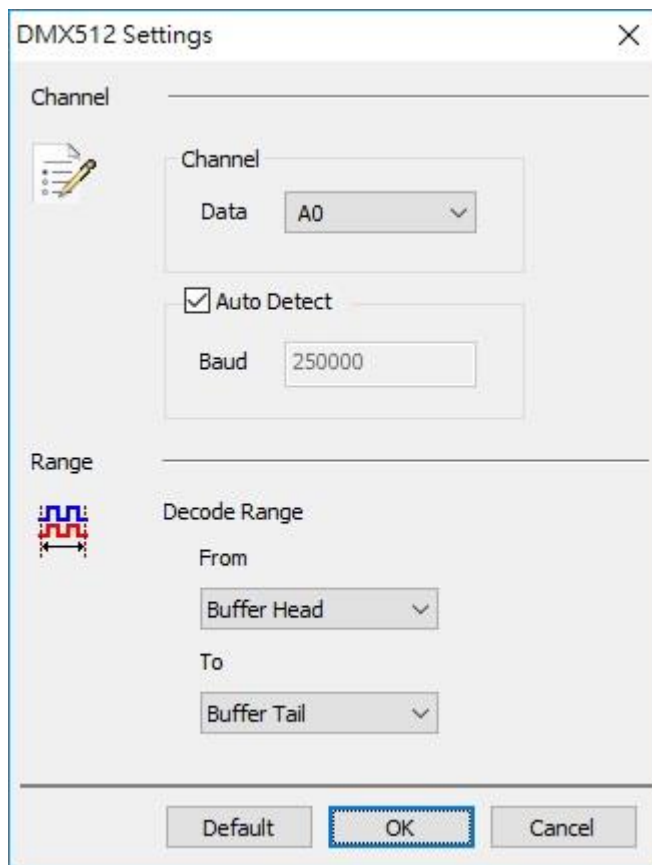
Response data



DMX512

DMX512 is a standard for digital communication networks that are commonly used to control stage lighting and effects..

Settings



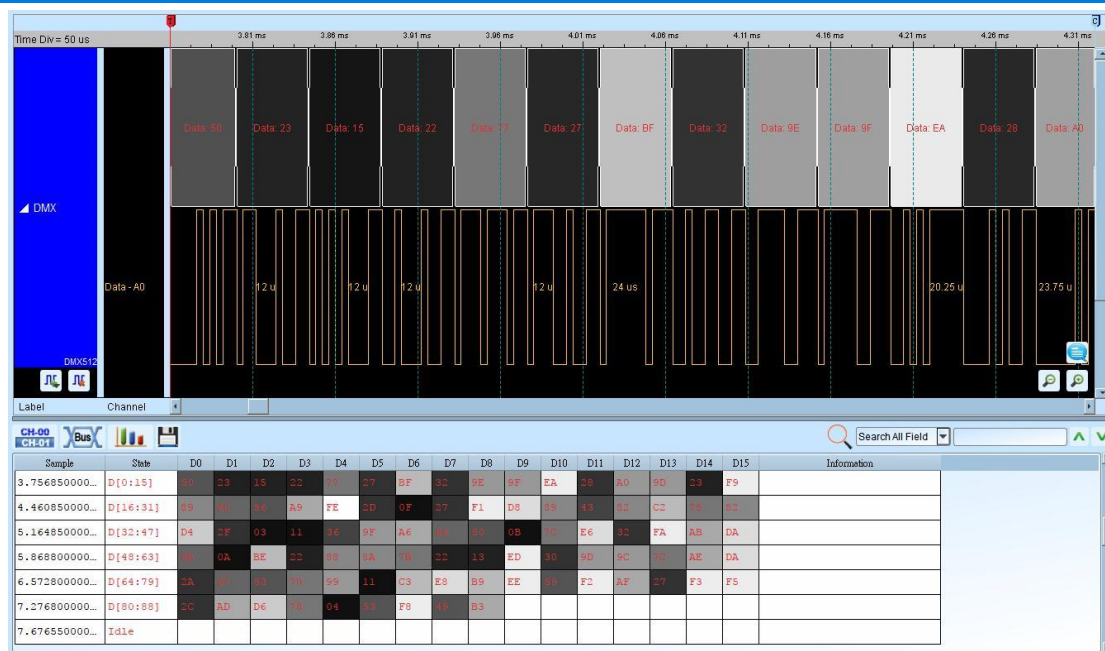
The image shows a 'DMX512 Settings' dialog box. It has a title bar with a close button (X). The dialog is divided into two main sections: 'Channel' and 'Range'. The 'Channel' section has a 'Data' dropdown menu set to 'A0' and a checked 'Auto Detect' checkbox. Below it is a 'Baud' text field containing '250000'. The 'Range' section has a 'Decode Range' label, a 'From' dropdown set to 'Buffer Head', and a 'To' dropdown set to 'Buffer Tail'. At the bottom are three buttons: 'Default', 'OK' (which is highlighted with a blue border), and 'Cancel'.

Data: Show the selected channel (CH0).

Auto Detect: Set the Baud Rate manually if not selected.

Result

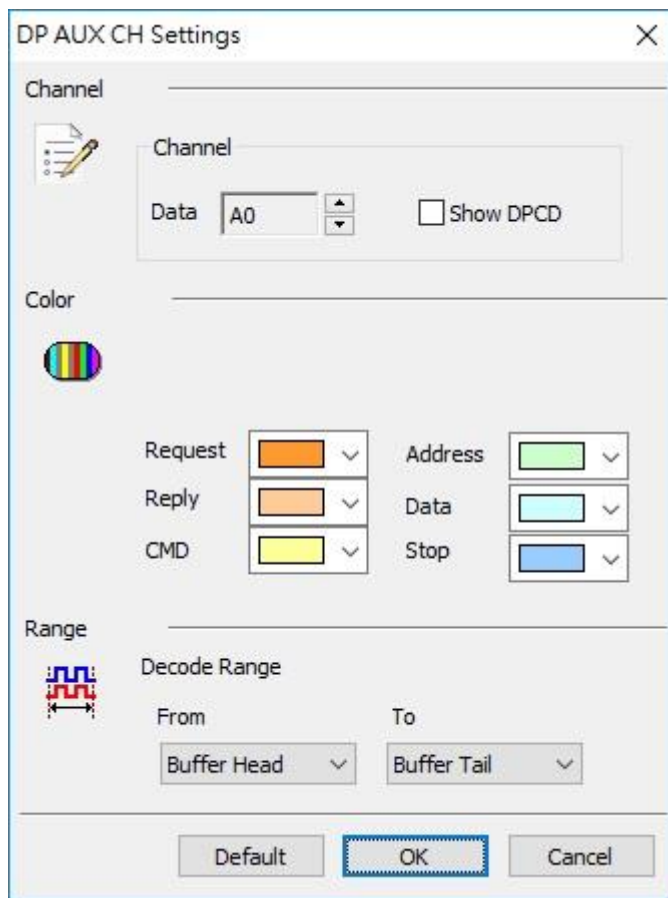
Use grayscale to display the decode results.



Display Port Auxiliary Channel (DP Aux Ch)

The DP Aux Ch is to detect the link, configuration and status of the Display Port source. The Display Port is the digital display interface that is specified in the VESA standard.

Settings



The image shows a 'DP AUX CH Settings' dialog box with a close button (X) in the top right corner. The dialog is divided into three main sections: Channel, Color, and Range.

- Channel Section:** Contains a 'Channel' label, a 'Data' dropdown menu currently set to 'A0', and an unchecked checkbox labeled 'Show DPCD'.
- Color Section:** Features a color calibration icon (a circle with vertical bars of different colors). Below it are two columns of color selection dropdowns:
 - Left column: 'Request' (orange), 'Reply' (light orange), and 'CMD' (yellow).
 - Right column: 'Address' (light green), 'Data' (light blue), and 'Stop' (blue).
- Range Section:** Includes a 'Range' label and a 'Decode Range' section with 'From' and 'To' dropdowns, both currently set to 'Buffer Head' and 'Buffer Tail' respectively.

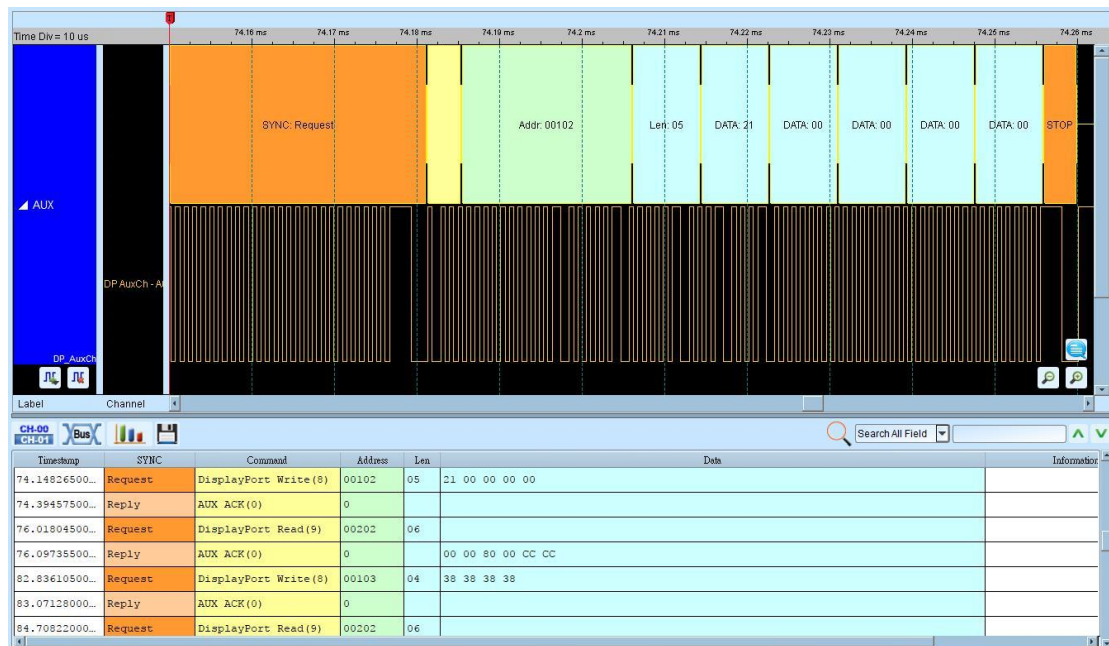
At the bottom of the dialog are three buttons: 'Default', 'OK' (which is highlighted with a blue dashed border), and 'Cancel'.

Data: Show the selected channel (CH0).

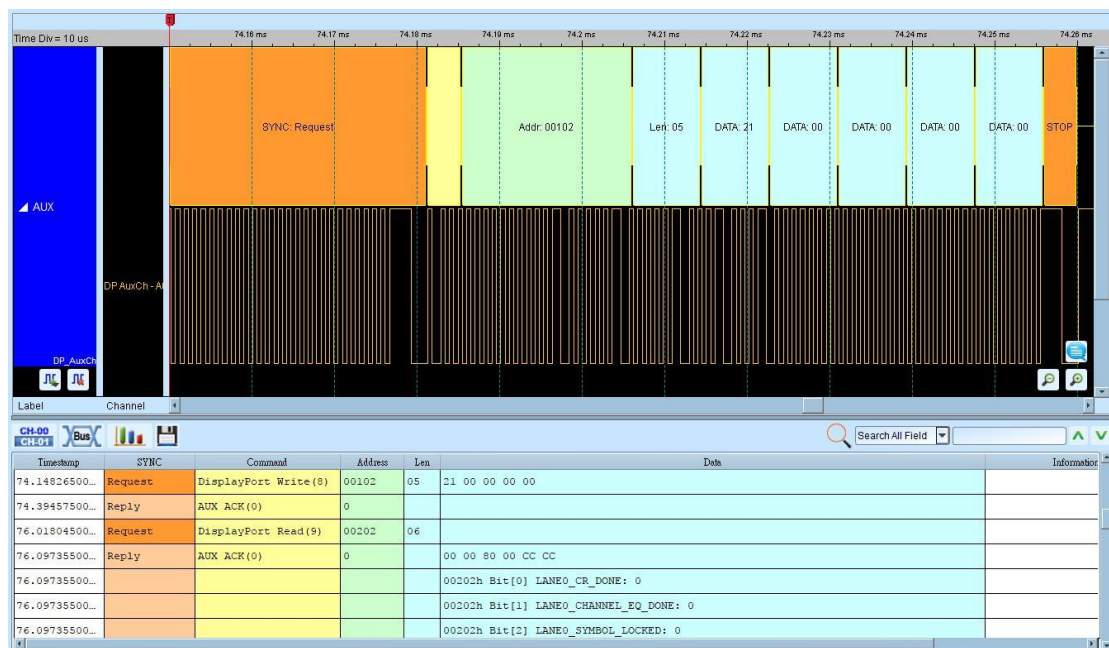
Show DPCD: Show the Display Port Configuration data.

Result

Without the DPCD information



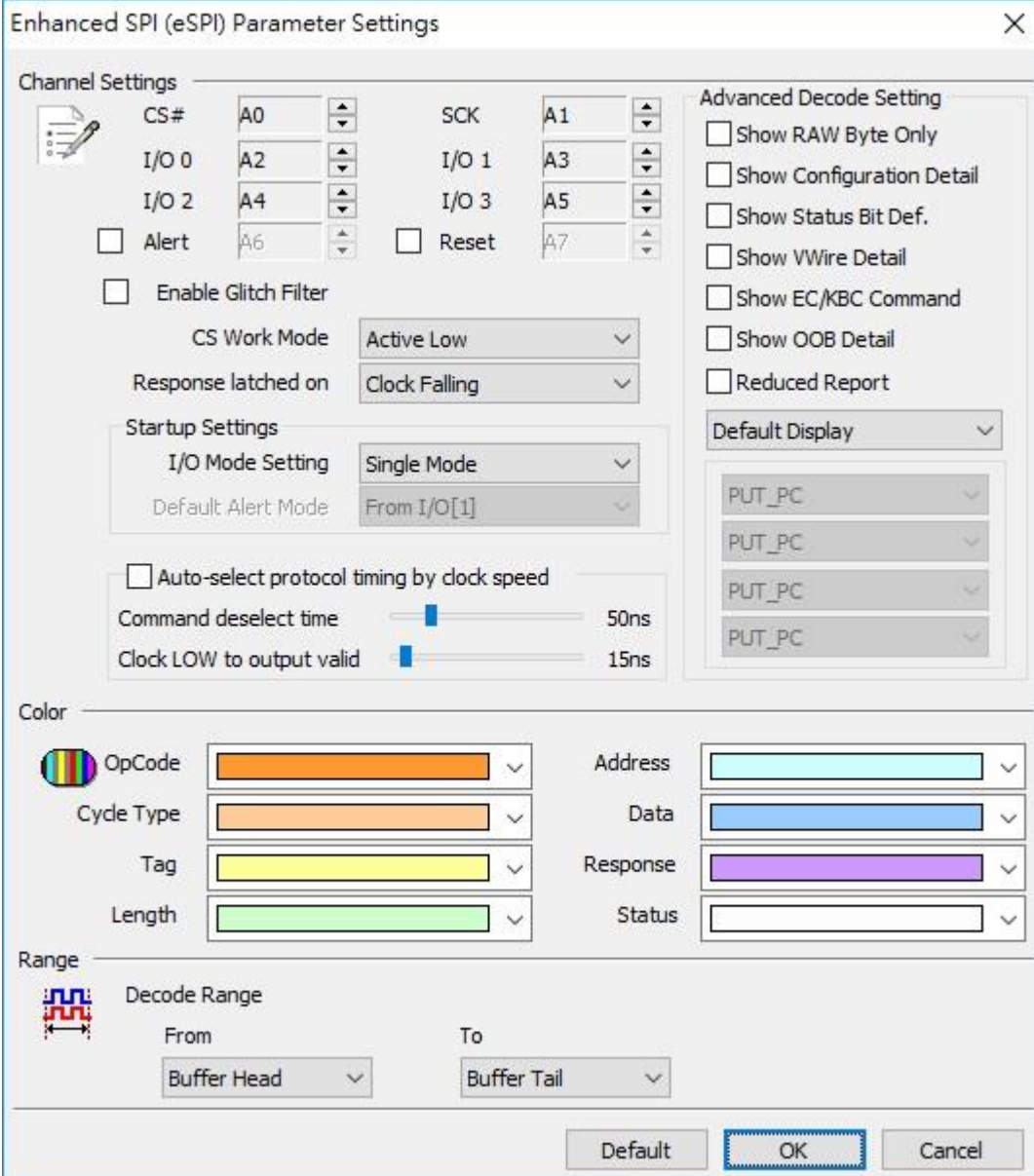
Show the DPCD information



Enhanced Serial Peripheral Interface (eSPI)

eSPI is the transmission protocol used in new generation baseboard of Intel, and its specification is to integrate SMBus / LPC / SPI Flash interface to simplify bus and increase transmission efficiency. Source of specification is based on Enhanced Serial Peripheral Interface (eSPI) Interface Base Specification (for Client and Server Platforms) June 2013, Revision 0.75.

Settings



The dialog box is titled "Enhanced SPI (eSPI) Parameter Settings" and contains several sections for configuring the interface.

Channel Settings

- CS#: A0, A1, A2, A3, A4, A5, A6, A7 (dropdowns)
- SCK: A1 (dropdown)
- I/O 0: A2 (dropdown)
- I/O 1: A3 (dropdown)
- I/O 2: A4 (dropdown)
- I/O 3: A5 (dropdown)
- Alert: ☐ (checkbox)
- Reset: ☐ (checkbox)
- Enable Glitch Filter: ☐ (checkbox)
- CS Work Mode: Active Low (dropdown)
- Response latched on: Clock Falling (dropdown)
- Startup Settings
 - I/O Mode Setting: Single Mode (dropdown)
 - Default Alert Mode: From I/O[1] (dropdown)
- Auto-select protocol timing by clock speed: ☐ (checkbox)
- Command deselect time: 50ns (slider)
- Clock LOW to output valid: 15ns (slider)

Advanced Decode Setting

- Show RAW Byte Only: ☐ (checkbox)
- Show Configuration Detail: ☐ (checkbox)
- Show Status Bit Def.: ☐ (checkbox)
- Show VWire Detail: ☐ (checkbox)
- Show EC/KBC Command: ☐ (checkbox)
- Show OOB Detail: ☐ (checkbox)
- Reduced Report: ☐ (checkbox)
- Default Display: (dropdown)
- PUT_PC (dropdown)
- PUT_PC (dropdown)
- PUT_PC (dropdown)
- PUT_PC (dropdown)

Color

- OpCode: (color bar)
- Cycle Type: (color bar)
- Tag: (color bar)
- Length: (color bar)
- Address: (color bar)
- Data: (color bar)
- Response: (color bar)
- Status: (color bar)

Range

- Decode Range
 - From: Buffer Head (dropdown)
 - To: Buffer Tail (dropdown)

Buttons: Default, OK, Cancel

Channel:

CS#: Chip Select (Active Low)

SCK: Clock

I/O0 – I/O3: Data input / output

Alert: Alert signal (Optional)

Startup Settings:

I/O Mode Setting: Set the initial I / O state to be Single / Dual / Quad, and I / O state would be switched automatically by the content of the waveform.

Default Alert Mode: Set the channel of Alert signal.

Command deselect time: Set tSHSL, Chip Select# Deassertion Time.

Clock LOW to output valid: Set tCLQV, Output Data Valid Time.

Advanced Decode Setting:

Show Configuration Detail: Show details of SET_CONFIG / GET_CONFIG.

Show Status Bit Def.: Show details of Status.

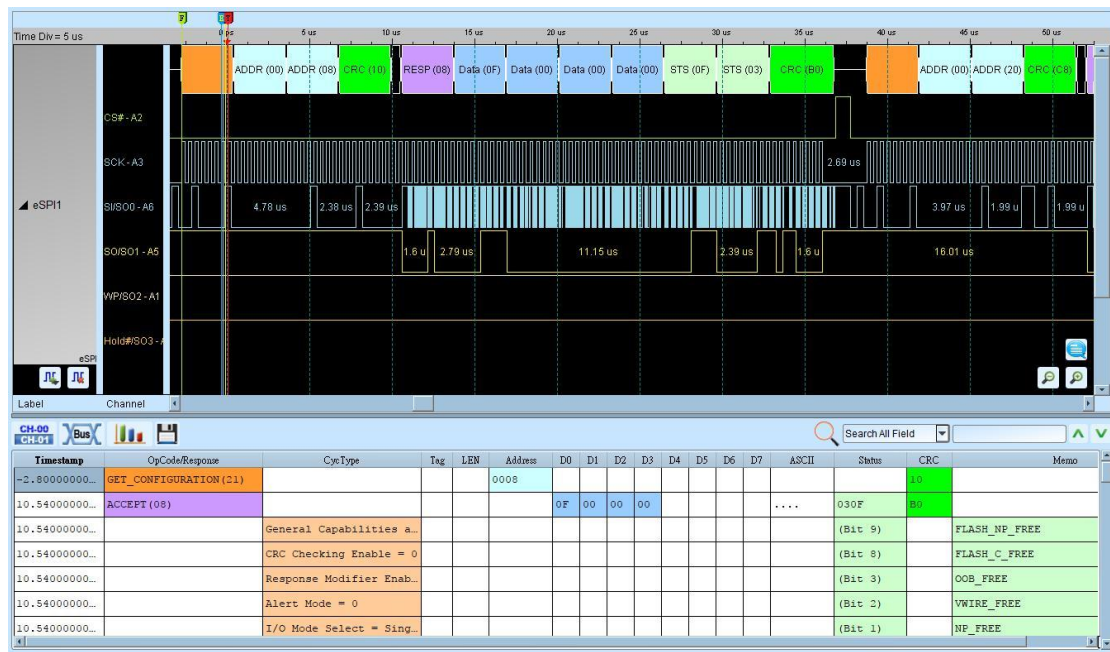
Reduced Report: Reducing the report is easy to check the Command Flow.

Filter Setting: To show or hide the specific OP Code / Cycle Type or Address range in the report.

Note: The setting of Address Filter would be saved as LA\eSPI\eSPIFilterX.bin in the work directory.

Result

Click **OK** to run the eSPI decode and see the result on the Waveform Window below.



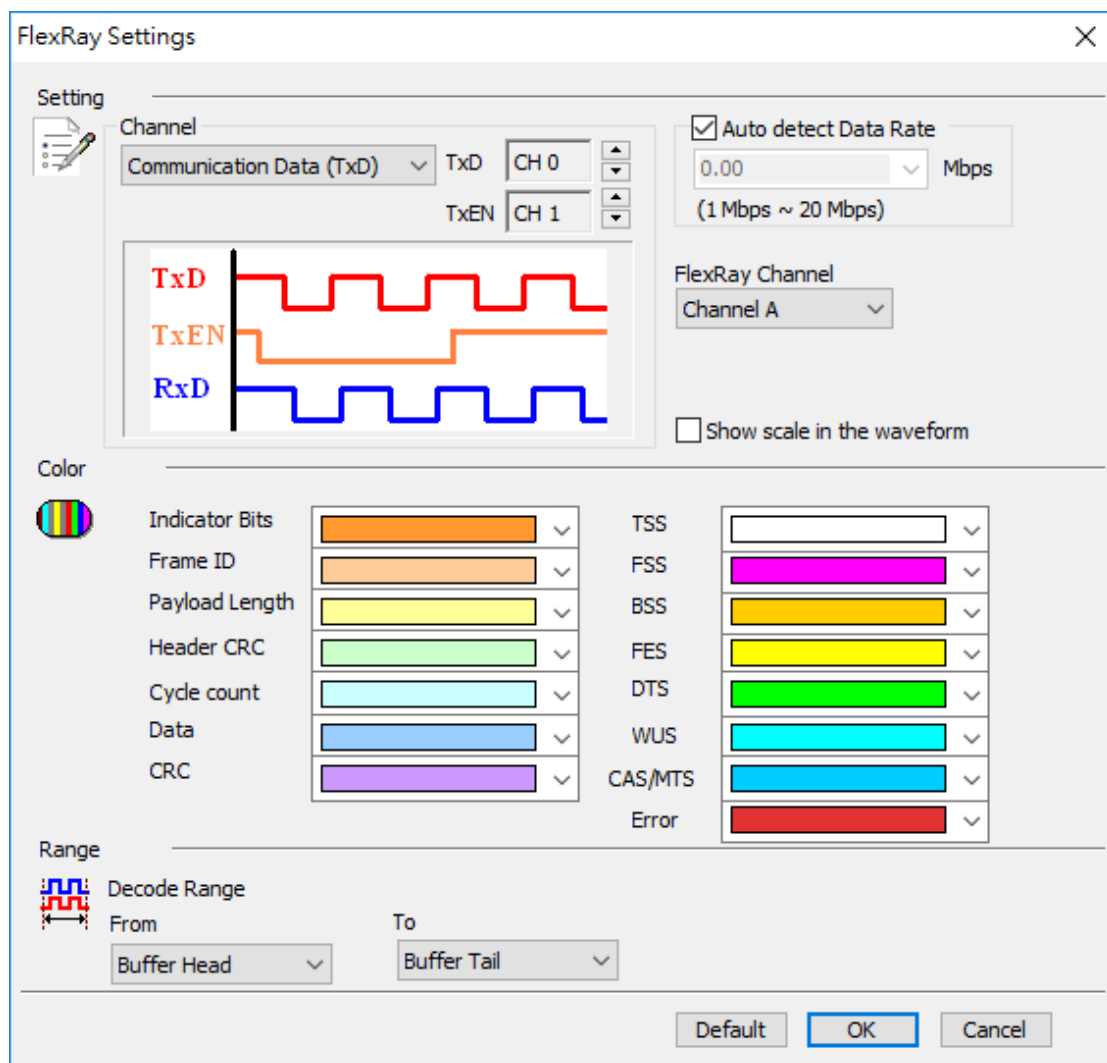
FlexRay

The FlexRay protocol has 2 bits with timing at 10Mbps.

FlexRay signal

Communication Data Layer: The FlexRay communication data is either at transmitter (TxD) or receiver (RxD) of the FlexRay transceiver. You may set the threshold according to the FlexRay transceiver voltage.

Settings



The FlexRay Settings dialog box is divided into several sections:

- Setting:** Includes a Channel dropdown set to "Communication Data (TxD)", TxD and TxEN channel selectors (CH 0 and CH 1), an "Auto detect Data Rate" checkbox (checked), a data rate input field (0.00 Mbps), and a FlexRay Channel dropdown (Channel A). A "Show scale in the waveform" checkbox is also present.
- Color:** A color palette icon is followed by two columns of color selection dropdowns. The first column includes Indicator Bits (orange), Frame ID (light orange), Payload Length (yellow), Header CRC (light green), Cycle count (light blue), Data (blue), and CRC (purple). The second column includes TSS (white), FSS (magenta), BSS (yellow), FES (yellow), DTS (green), WUS (cyan), CAS/MTS (cyan), and Error (red).
- Range:** A waveform icon is followed by a "Decode Range" section with "From" and "To" dropdowns, both set to "Buffer Head" and "Buffer Tail" respectively.

At the bottom right are buttons for "Default", "OK", and "Cancel".

Channel: Display the channel, Physical Layer is the default.

Communication Data (TxD): The TxD data is from the TxD and TxEN of the FlexRay transceiver.

Communication Data (RxD): The RxD data is from the RxD and RxEN of the FlexRay transceiver.

Auto detect Data Rate: Default is Auto Bit Rate. If disabled, you may use built-in Bit Rate 10/5/2.5 Mbps or input manually, ranges from 1Mbps-20Mbps.

FlexRay Channel: Channel A or B, for Frame CRC checking.

Errors are:

Error	Description
TSS Error	Unable to detect TSS
FSS Error	Unable to detect FSS
BSS Error	Unable to detect BSS
FES Error	Unable to detect FES
Header CRC Error	The header CRC value is incorrect
Frame CRC Error	The frame CRC value is incorrect

Abbreviations are:

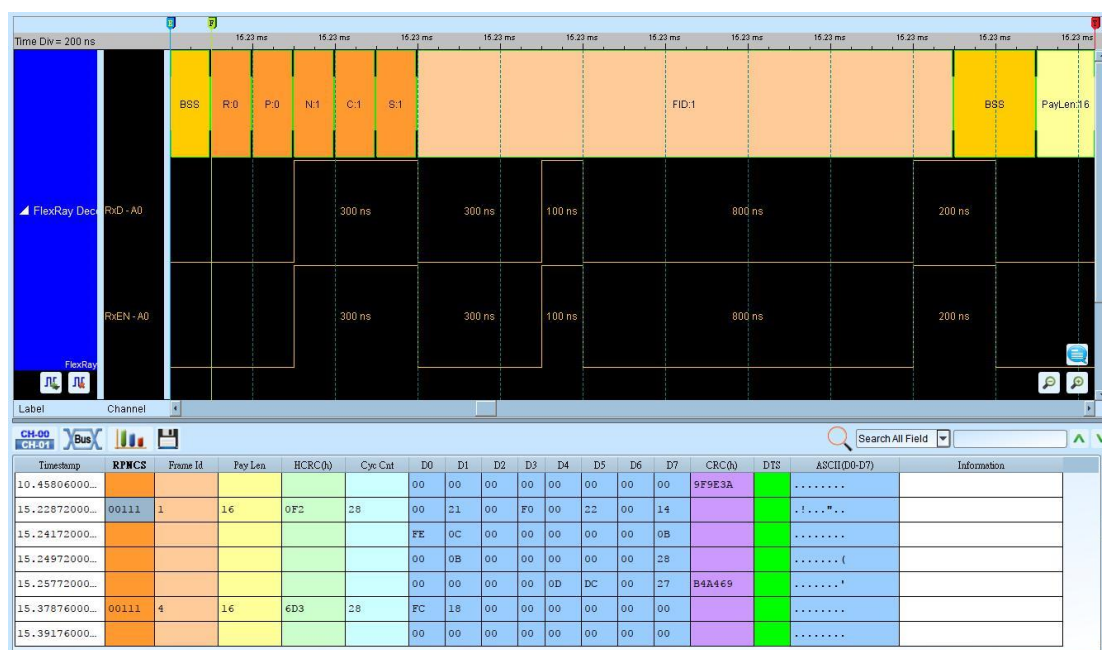
Abbreviation	Description
TSS	Transmission start sequence
FSS	Frame start sequence
BSS	Byte start sequence
FES	Frame end sequence
DTS	Dynamic trailing sequence
CAS	Collision Avoidance Symbol
MTS	Media Access Test Symbol

WUP	Wakeup Pattern
CID	Channel Idle Delimiter

Result

Click **OK** to run the FlexRay decode and see the result on the Waveform Window below.

10Mbps FlexRay Communication Data(RxD)



HD Audio

High Definition Audio, also known as HD Audio or by its codename, Azalia, is an audio standard created by Intel to be used on their chipsets, i.e., it is a standard for high-quality on-board audio. In this tutorial we will explain more about this feature.

Settings

HD Audio Settings

Channel

SYNC A0 I/O 0 A2 Direction ☒ SDI ☐ SDO

BCLK A1

Color

Stream Data

Preamble [Color Picker] Stream ID [Color Picker]

Length [Color Picker] Sample [Color Picker]

Response (SDI)

Valid [Color Picker] UnSol [Color Picker]

Reserved [Color Picker] Response [Color Picker]

Command (SDO)

Reserved [Color Picker] CAd [Color Picker]

NID [Color Picker] Verb ID [Color Picker]

Payload [Color Picker]

Range

Decode Range

From Buffer Head To Buffer Tail

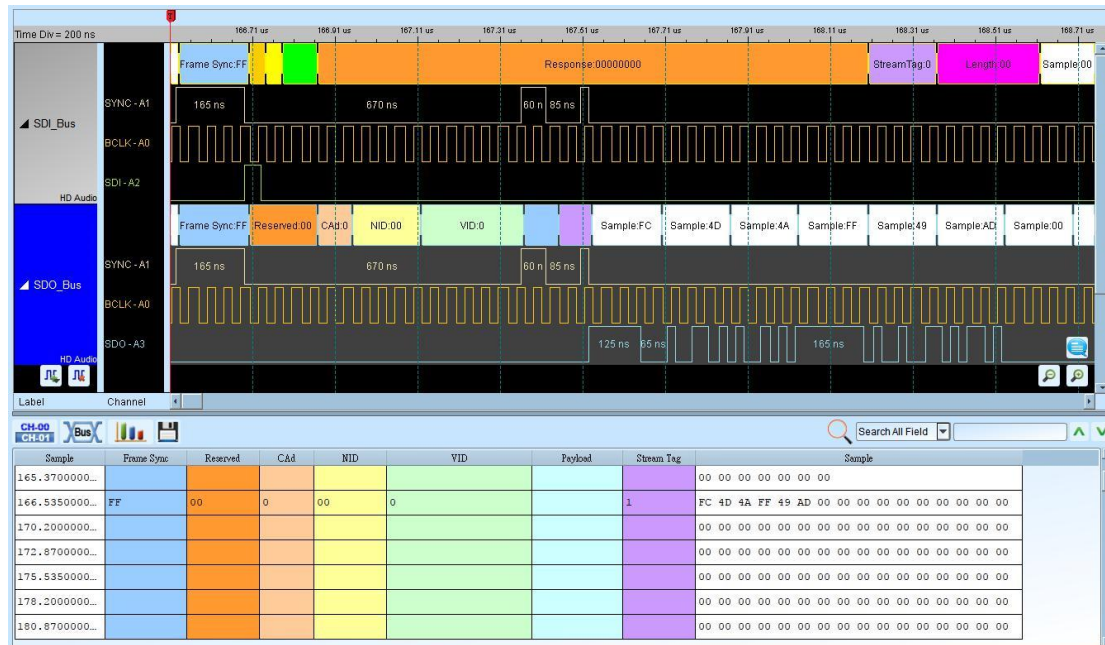
Default OK Cancel

Channel: Show the selected channel (CH 0-CH3).

Direction: Show the data with SDI or SDO decoding.

Result

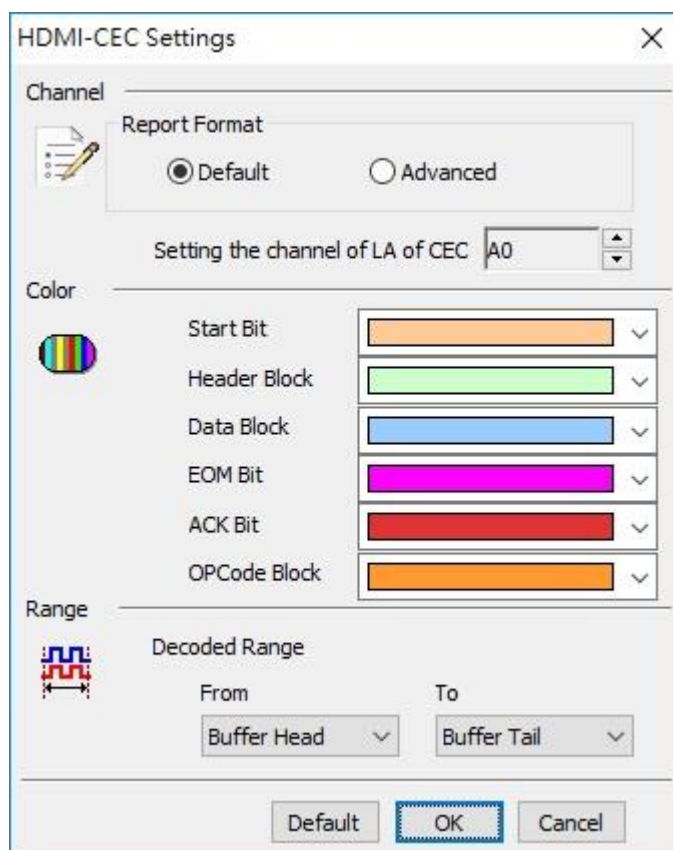
Click **OK** to run the HD Audio decode and see the result on the Waveform Window below.



HDMI-CEC

The HDMI-CEC bus is a one-wire, “party line” that connects up to ten (10) AV devices through standard HDMI cabling. The CEC protocol includes automatic mechanisms for physical address (topology) discovery, (product type based) logical addressing, arbitration, retransmission, broadcasting, and routing control. Message opcodes support both device specific (e.g. set-top-box, DTV, and player) and general features (e.g. for power, signal routing, remote control pass-through, and on-screen display).

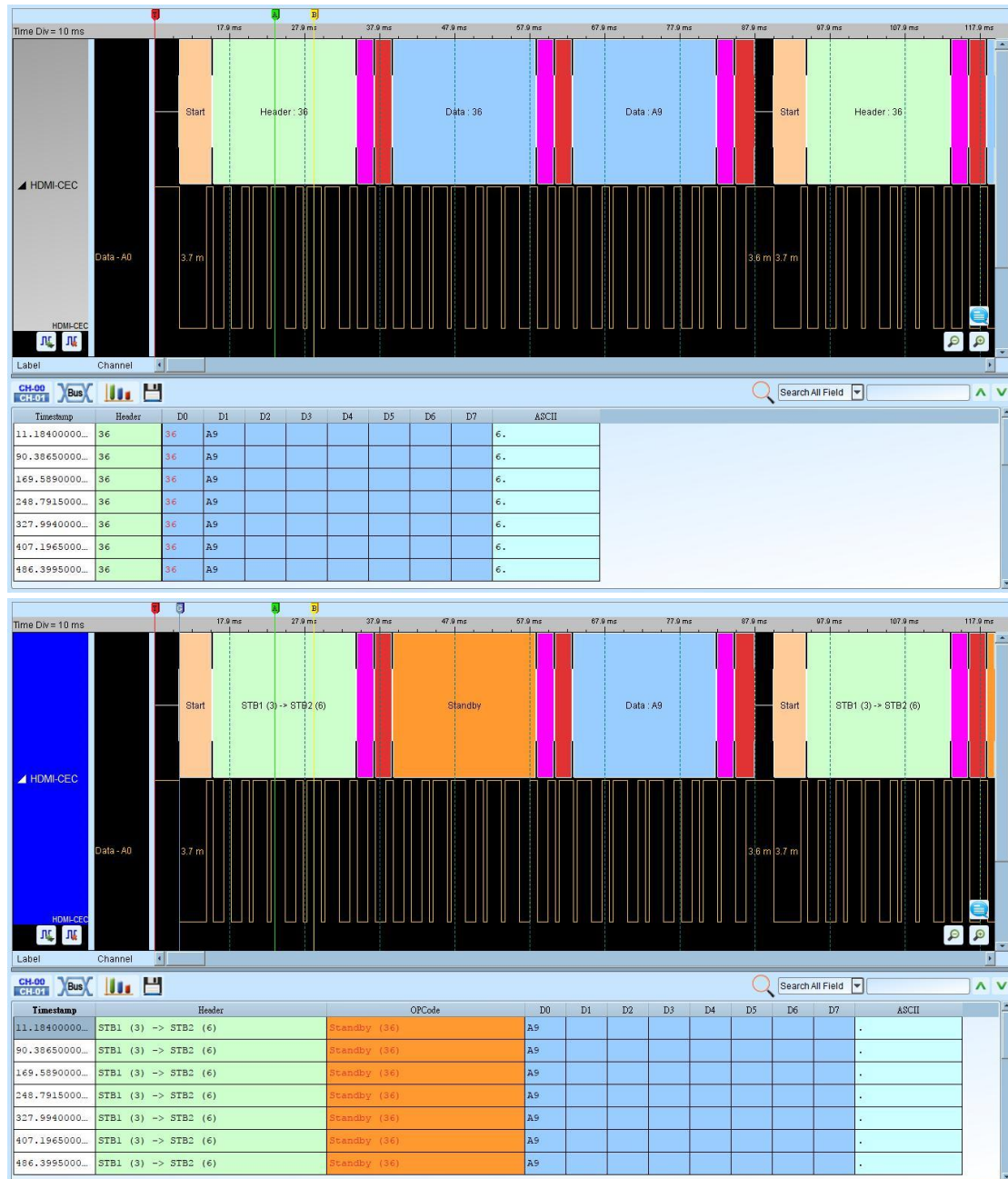
Settings



Latch data: Nominal (1.05 micro seconds) or User Define.

Result

Click **OK** to run the HDMI-CEC decode and see the result on the Waveform Window below.



HDMI-DDC (EDID)

EDID (Extended Display Identification Data) is I2C protocol base on DDC wire and transmitted monitor information. Now, HDMI, DVI and VGA are support this protocol.

Settings

DDC(EDID) Setting

Parameter Setting

Channel Setting

SCL A0 SDA A1

Address Mode

☒ 7-Bit Addressing

☐ 7-Bit Addressing(Include R/W in address)

☐ Ignore glitch ☐ Statistics Mode

Color

Start Stop Address Data Read/Write ACK NACK

Range

Decode Range

From to

Buffer Head Buffer Head

Default OK Cancel

Channel: Display the channels (CH0 and CH1).

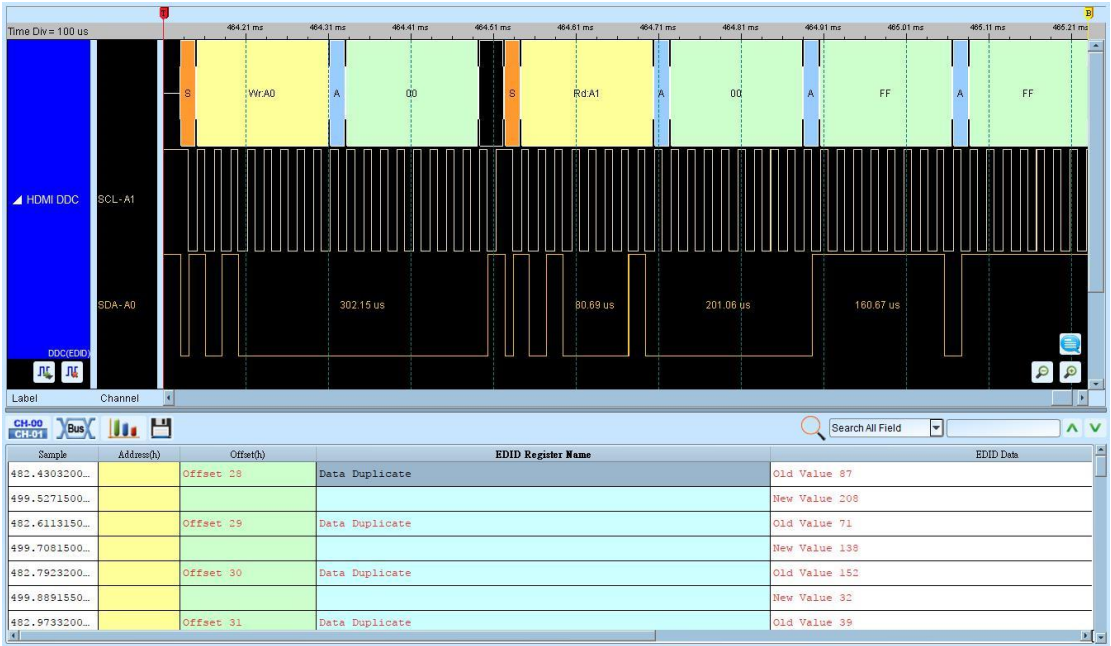
7-bit addressing: Show 7-bit addressing

7-bit addressing(Include R/W in Address): Show 8-bit addressing(include 7-bit addressing and 1-bit Rd/Wr).

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Statistic Mode: Collect all the data frames into one report by register address order.

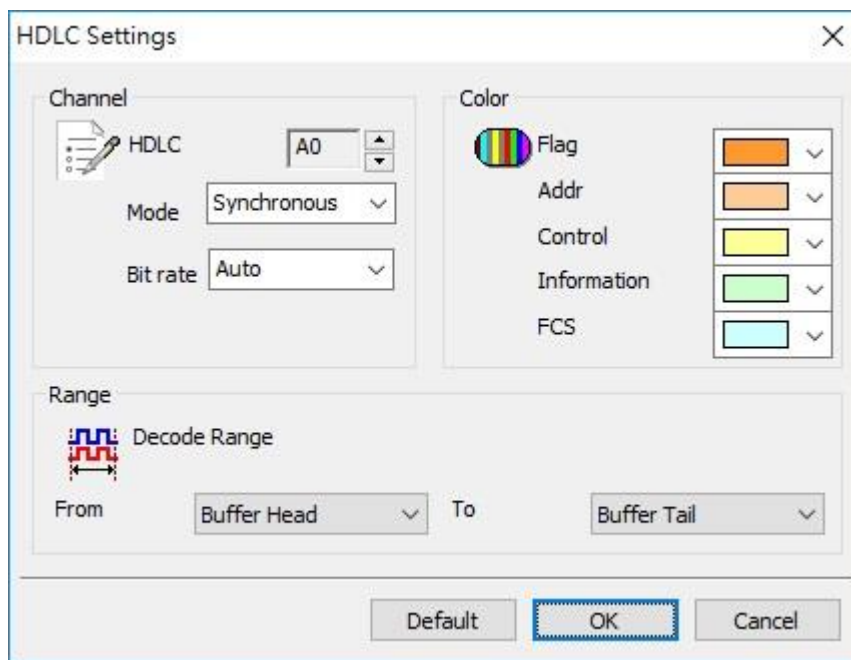
Result



HDLC

HDLC (High-level Data Link Control) is the default synchronous data link layer protocol used in the equipment of Cisco.

Settings

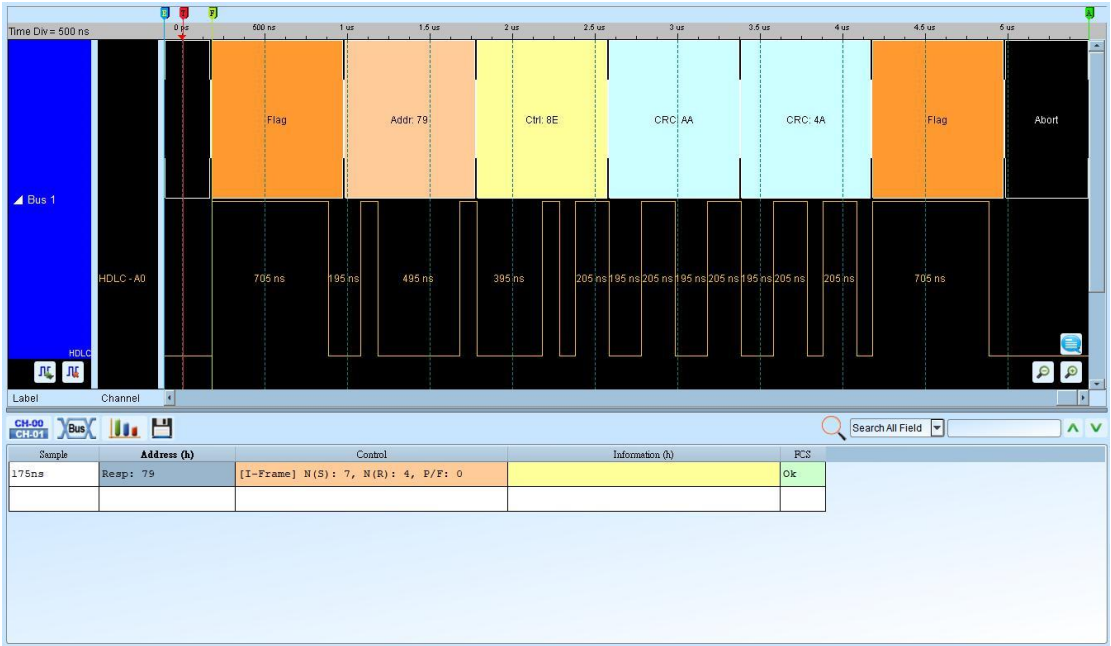


HDLC: Set the channel of the signal.

Mode: Synchronous or Asynchronous mode.

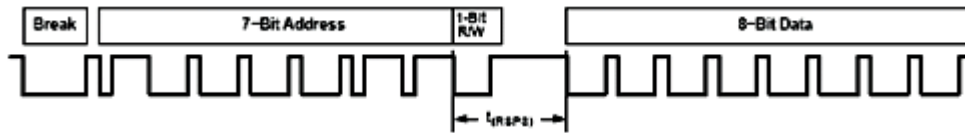
Bit rate: Set the specific data rate or auto detection.

Result

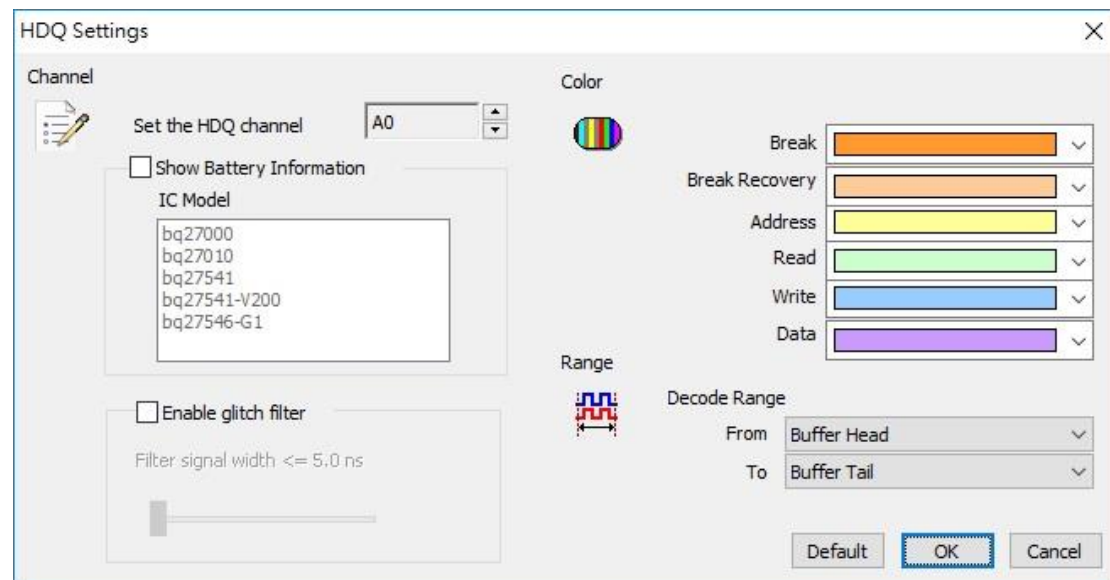


HDQ

The HDQ bus has two kinds of formats: 8 bits or 16 bits signals as the diagram below.



Settings

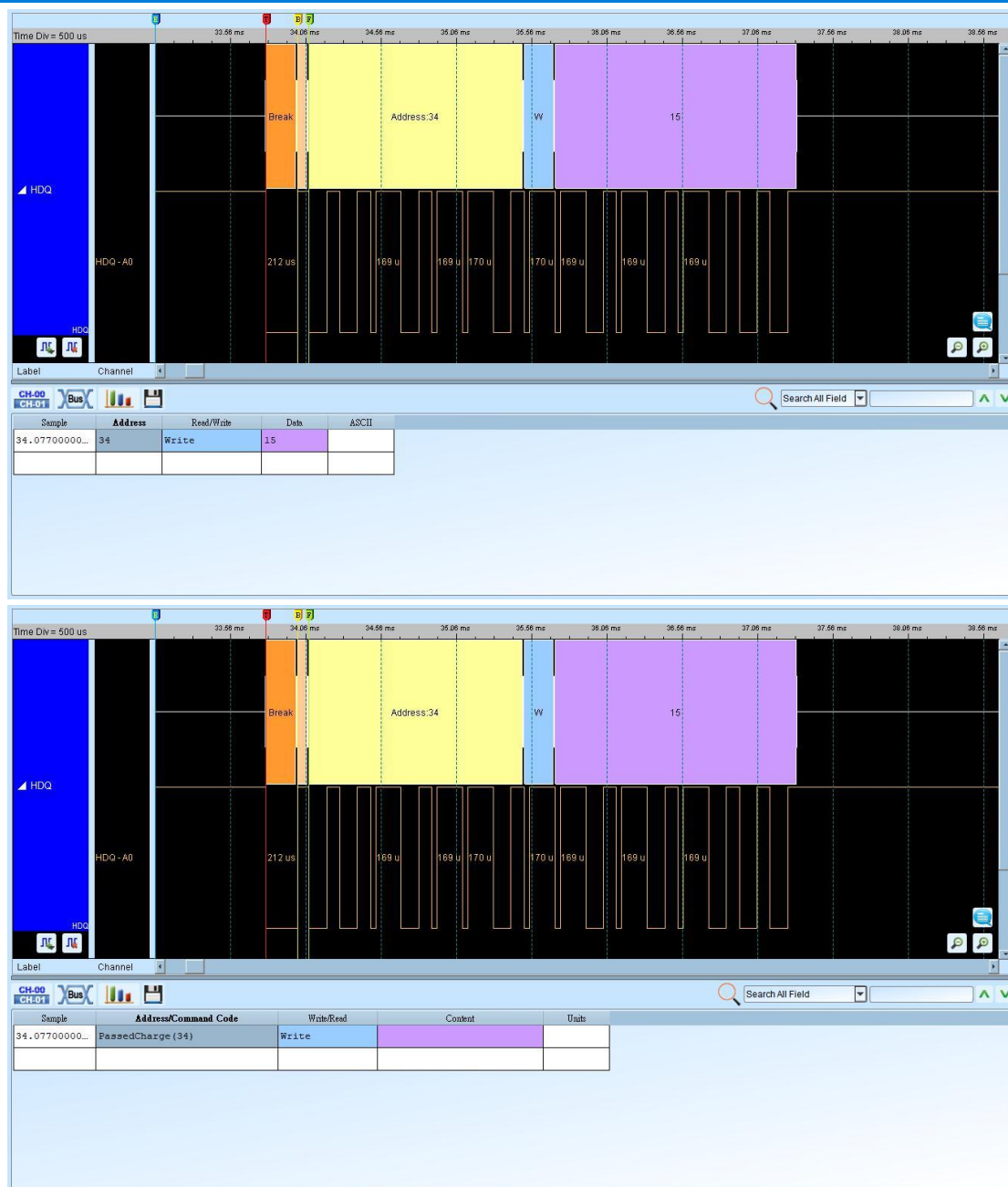


Channel: Set the HDQ channel: Show the selected channel (CH 0).

Show Battery Information: monitor the command between battery and IC.

Result

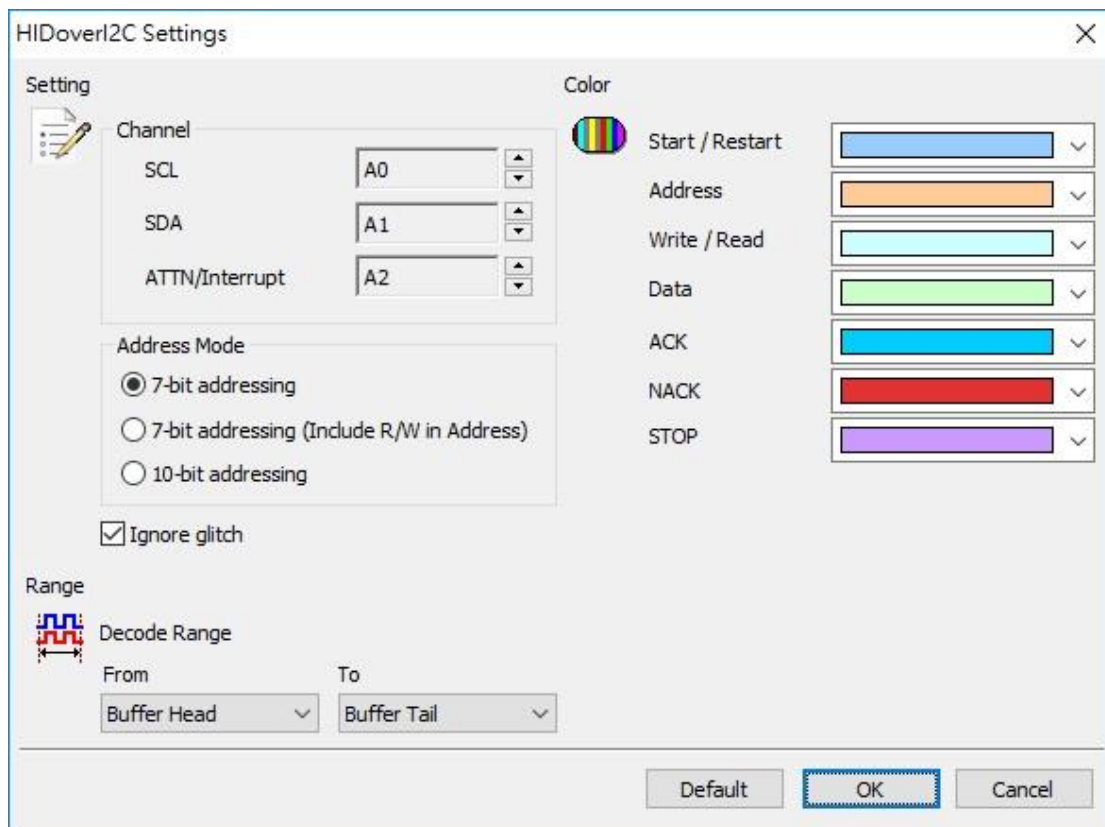
Click **OK** to run the HDQ decode and see the result on the Waveform Window below.



HID Over I²C

HID Over I2C (Human Interface Device Over I2C) protocol is established by Microsoft. It's applied for Windows 8 ARM platform.

Settings



Channel: Show the selected channels (SCL:CH0, SDA:CH1, ATTN:CH2).

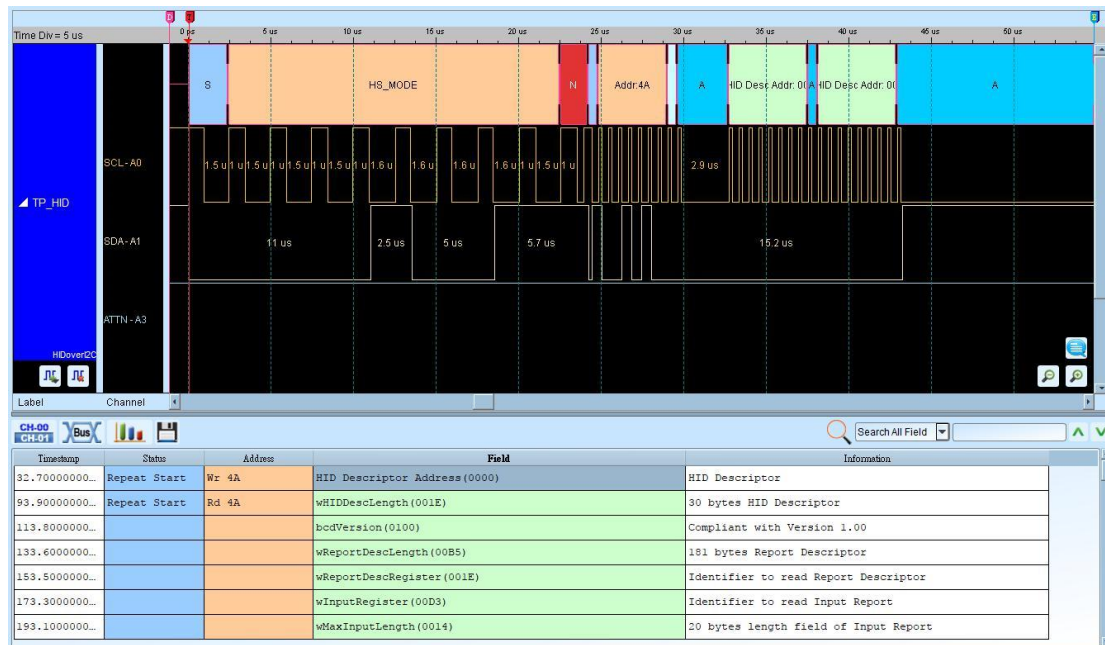
7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

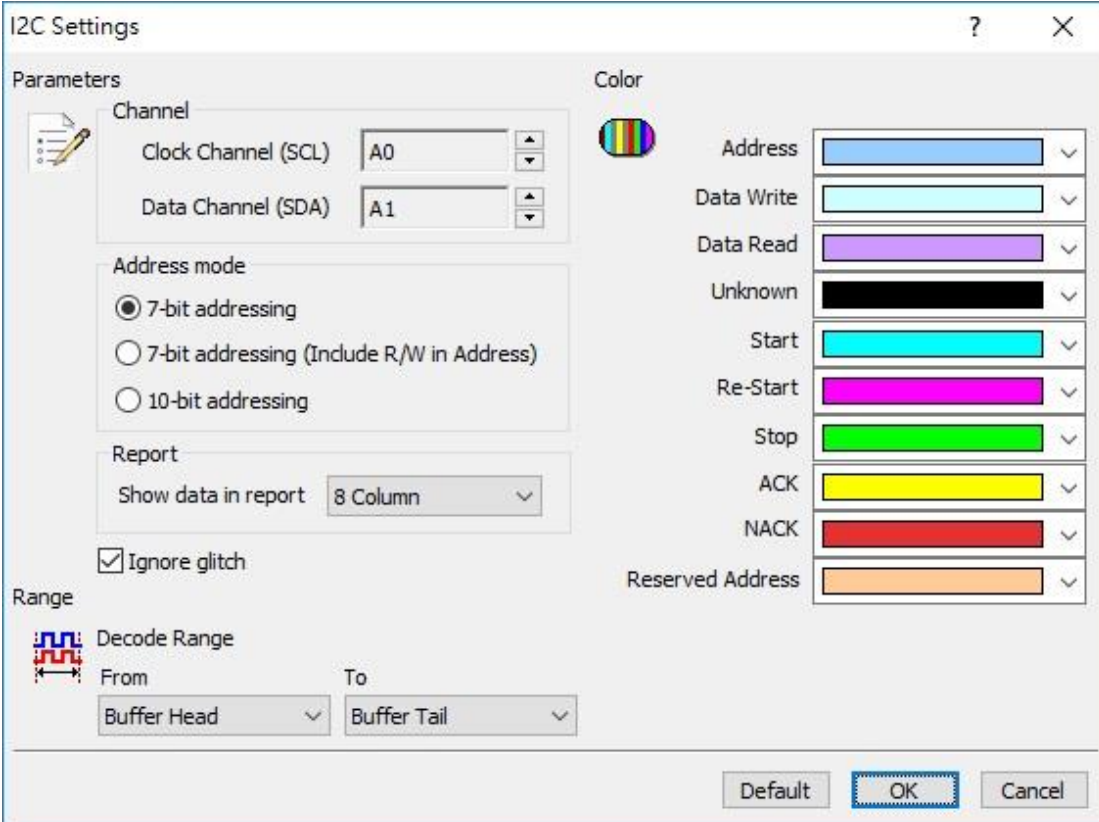
Result



I²C

The Inter-Integrated Circuit (I²C) bus has two data bits: Serial Data (SDA) and Serial Clock (SCL).

Settings



The I2C Settings dialog box is divided into two main sections: Parameters and Color. The Parameters section on the left includes a Channel section with dropdowns for Clock Channel (SCL) set to A0 and Data Channel (SDA) set to A1. Below this is the Address mode section with three radio buttons: 7-bit addressing (selected), 7-bit addressing (Include R/W in Address), and 10-bit addressing. The Report section has a dropdown for 'Show data in report' set to '8 Column' and a checked checkbox for 'Ignore glitch'. The Range section at the bottom left features a 'Decode Range' icon and two dropdowns for 'From' (Buffer Head) and 'To' (Buffer Tail). The Color section on the right, titled 'Color' with a rainbow icon, contains a list of color-coded events: Address (blue), Data Write (cyan), Data Read (purple), Unknown (black), Start (light blue), Re-Start (magenta), Stop (green), ACK (yellow), NACK (red), and Reserved Address (orange). Each event has a corresponding color swatch and a dropdown arrow. At the bottom right are buttons for 'Default', 'OK', and 'Cancel'.

Channel: Display the channels (CH0 and CH1).

Address Mode: Select the 7-bit or 10-bit address.

7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Report: Show either 8 or 16-columns data in the report window.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Result

Click **OK** to run the I²C decode and see the result on the Waveform Window below.

It shows frequency in the Information field.



I²C EEPROM

EEPROM can be erased and reprogrammed (written to) repeatedly through the application of higher than normal electrical voltage generated externally or internally in the case of modern EEPROMs.

Settings

I2C(EEPROM 24 Series) Settings

Parameters

Channel

Clock Channel (SCL) A0

Data Channel (SDA) A1

Address

Address Width 7

☐ 7-bit addressing (Include R/W in Address)

☐ 24LCS61 / 24LCS62

☒ Ignore glitch

Color

Start Output Enable

Control Device ID

Address Command Select

Read Data

Write Stop

ACK

NACK

Chip

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Channel: Display the channels (CH0 and CH1)

Address: The default address width is 7.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

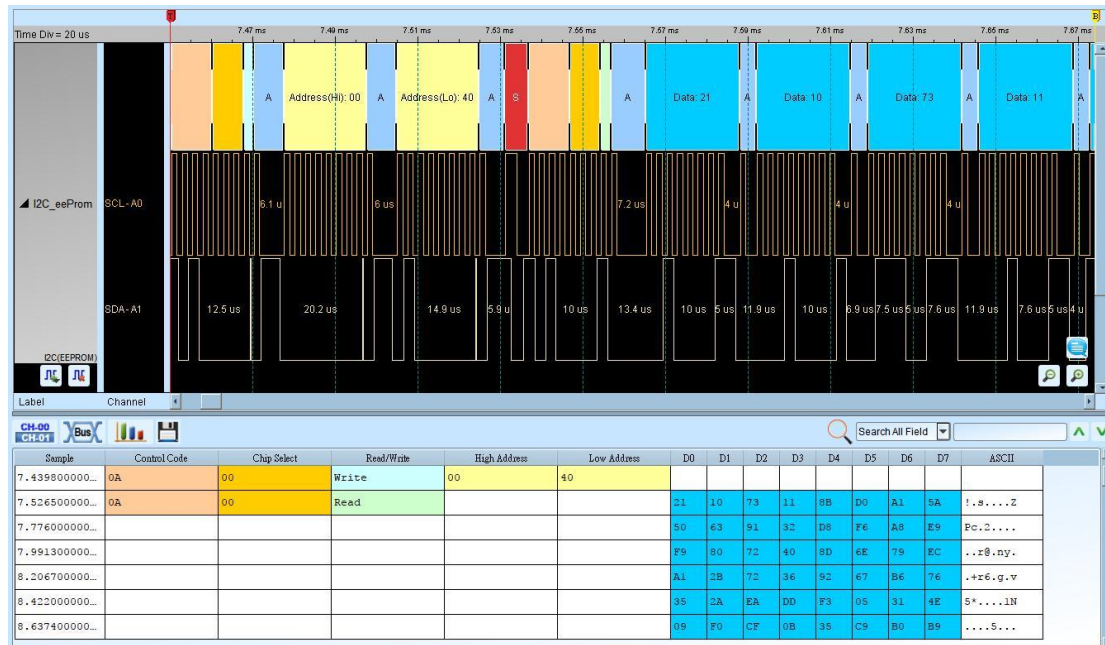
24LCS61/24LCS62: 24LCS61/24LCS62 EEPROM protocol.

Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click OK to run the I²C EEPROM decode and see the result on the Waveform

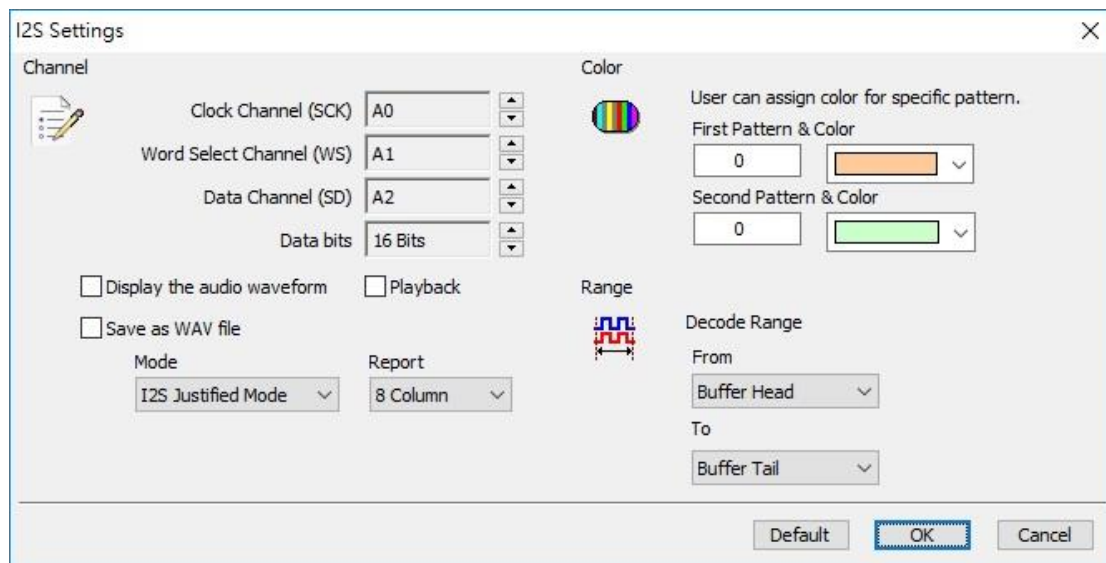
Window below.



I²S

The Inter-Integrated Circuit Sound (I²S) bus has three data bits: Serial Clock (SCK), Word Select Line (WS) and Multiplex Data Line (SD).

Settings



Channel: Show the selected channels (CH0, CH1 and CH2) and set Data bits (16 bits).

Display the audio waveform: Click to display the audio waveform in the Waveform Window.

Playback: Click to display the audio from the speaker..

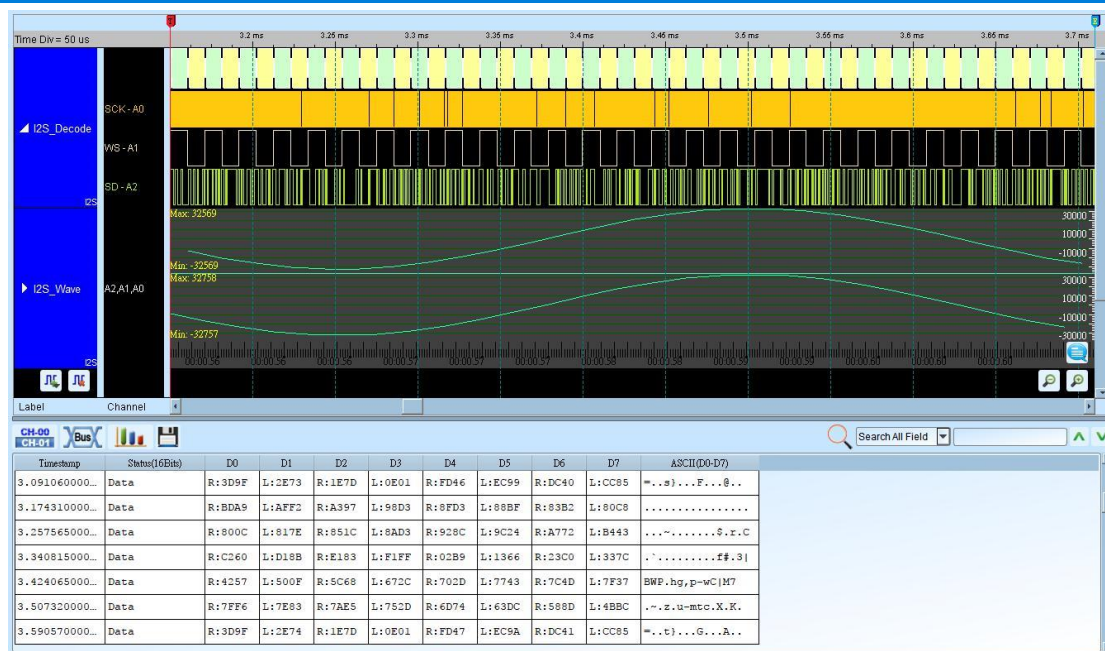
Save as WAV file: Click to save the data to a audio file(.wav) in the work directory.

Mode: I²S Justified/MSB Justified/LSB Justified/PCM/TDM.

Report: Select the column number.

Result


Click **OK** to run I²S decode and see the result on the Waveform Window below.



I80

The I80 controls 3 or 4-pins (WR, RD, CS, D/C) data.

Settings



The I80 Settings dialog box is divided into four main sections: Channel, Color, Range, and buttons at the bottom.

- Channel Section:** Contains a 'Select Channel' area with a grid of address inputs (A0-A23) for channels WR, RD, CS, and D/C. Below this are three dropdown menus: 'Data Bus' (empty), 'Bit Order' (set to 'LSB First'), and 'Report Data' (set to '8 Column').
- Color Section:** Contains a 'Setting Color' area with four color pickers: 'Command' (orange), 'Data' (light orange), 'Read' (yellow), and 'Write' (green).
- Range Section:** Contains a 'Decode Range' area with two dropdown menus: 'From' (set to 'Buffer Head') and 'To' (set to 'Buffer Tail').
- Buttons:** At the bottom are three buttons: 'Default', 'OK' (highlighted with a blue border), and 'Cancel'.

Select Channel: Show the selected channels (WR, RD, CS, D0, D1, D2, D3, D4, D5, D6,...).

On D/C: Use the D/C pin as Command (Low) or Data (High).

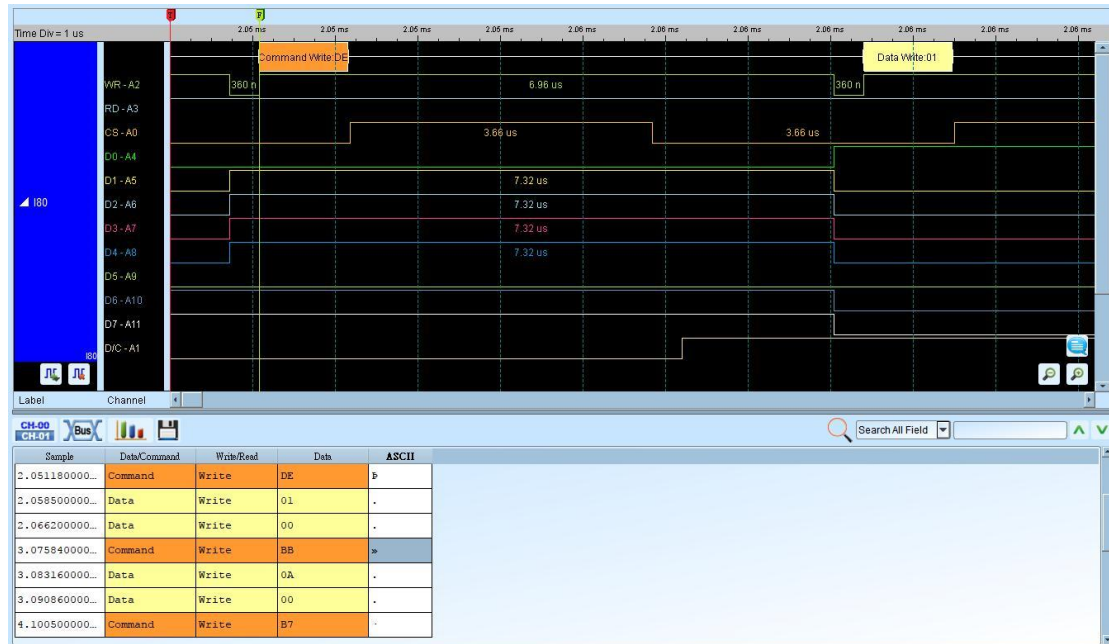
Data Bus: Select 4 Bit, 8 Bit, 12 Bit, 16 Bit, 20 Bit, or 24 Bit.

Bit Order: Select LSB First or MSB First.

Report Data: Select 8 columns or 16 columns.

Result

Click **OK** to run the I80 decode and see the result on the Waveform Window below.



IDE

IDE (Integrated Device Electronics) is a computer hardware bus and has the following data bits:

General Channel (11 pins): DASP-, DIOR-:HDMARDY-:HSTROBE, DIOW-:STOP, DMACK-, DMARQ, INTRQ, IORDY:DDMARDY-:DSTROBE, PDIAG-:CBLID-, RESET-, CSEL, IOCS16-.

Register Channel (5 pins): CS(0:1)-, DA(2:0).

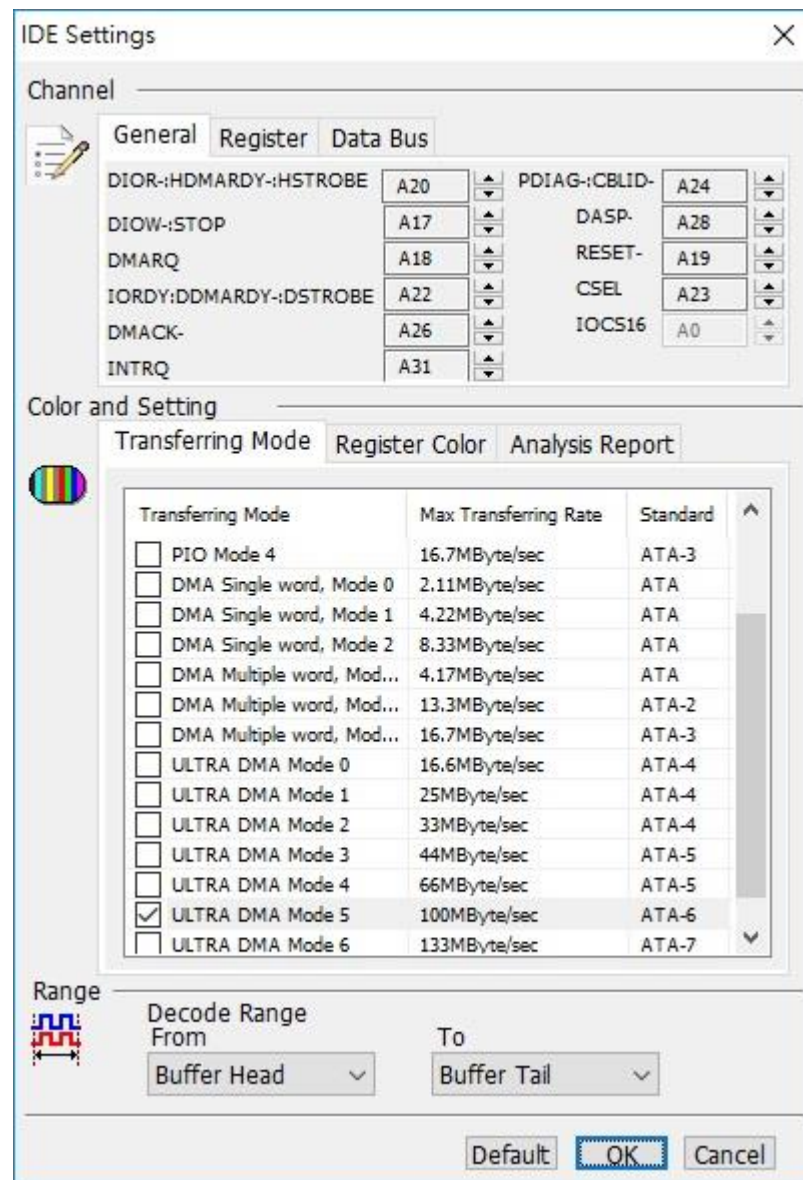
Data Bus (16 pins): DD(15:0)

We recommend that IDE bus of the target system to be connected to the instrument as the following table:

IDE Pin No.	IDE Pin name	IDE Pin Description	LA default Channel No.
Pin1	Reset-	Hardware reset	Channel 0
Pin2	Ground		
Pin3	DD7	Device data	Channel 1
Pin4	DD8	Device data	Channel 2
Pin5	DD6	Device data	Channel 3
Pin6	DD9	Device data	Channel 4
Pin7	DD5	Device data	Channel 5
Pin8	DD10	Device data	Channel 6
Pin9	DD4	Device data	Channel 7
Pin10	DD11	Device data	Channel 8
Pin11	DD3	Device data	Channel 9
Pin12	DD12	Device data	Channel 10
Pin13	DD2	Device data	Channel 11
Pin14	DD13	Device data	Channel 12
Pin15	DD1	Device data	Channel 13
Pin16	DD14	Device data	Channel 14

Pin17	DD0	Device data	Channel 15
Pin18	DD15	Device data	Channel 16
Pin19	Ground		
Pin20	Key pin		
Pin21	DMARQ	DMA request	Channel 17
Pin22	Ground		
Pin23	DIOW-:STOP	Device I/O write: Stop Ultra DMA burst	Channel 18
Pin24	Ground		
Pin25	DIOR-:HDMAR DY- :HSTROBE	Device I/O read: Ultra DMA ready: Ultra DMA data strobe	Channel 19
Pin26	Ground		
Pin27	IORDY:DDMAR DY- :DSTROBE	I/O channel ready: Ultra DMA ready: Ultra DMA data strobe	Channel 20
Pin28	CSEL	Cable select	Channel 21
Pin29	DMACK-	DMA acknowledge	Channel 22
Pin30	Ground		
Pin31	INTRQ	Device interrupt	Channel 23
Pin32	Obsolete (see note)	Device 16-bit I/O in ATA-2	Channel 24
Pin33	DA1	Device address	Channel 25
Pin34	PDIAG-:CBLID-	Passed diagnostics: Cable assembly type identifier	Channel 26
Pin35	DA0	Device address	Channel 27
Pin36	DA2	Device address	Channel 28
Pin37	CS0-	Chip select	Channel 29
Pin38	CS1-	Chip select	Channel 30
Pin39	DASP-	Device active, device 1 present	Channel 31
Pin40	Ground		

Settings



The IDE Settings dialog box is divided into two main sections: "Channel" and "Color and Setting".

Channel Section: This section contains three tabs: "General", "Register", and "Data Bus". The "General" tab is active, showing a list of hardware signals and their corresponding address ranges. The signals are arranged in two columns, each with a set of up and down arrows for adjustment.

Signal	Address
DIOR-:HDMARDY-:HSTROBE	A20
DIOW-:STOP	A17
DMARQ	A18
IORDY:DDMARDY-:DSTROBE	A22
DMACK-	A26
INTRQ	A31
PDIAG-:CBLID-	A24
DASP-	A28
RESET-	A19
CSEL	A23
IOCS16	A0

Color and Setting Section: This section contains three tabs: "Transferring Mode", "Register Color", and "Analysis Report". The "Transferring Mode" tab is active, showing a list of data transfer modes with their maximum rates and standards. A checkmark is placed next to "ULTRA DMA Mode 5".

Transferring Mode	Max Transferring Rate	Standard
<input type="checkbox"/> PIO Mode 4	16.7MByte/sec	ATA-3
<input type="checkbox"/> DMA Single word, Mode 0	2.11MByte/sec	ATA
<input type="checkbox"/> DMA Single word, Mode 1	4.22MByte/sec	ATA
<input type="checkbox"/> DMA Single word, Mode 2	8.33MByte/sec	ATA
<input type="checkbox"/> DMA Multiple word, Mod...	4.17MByte/sec	ATA
<input type="checkbox"/> DMA Multiple word, Mod...	13.3MByte/sec	ATA-2
<input type="checkbox"/> DMA Multiple word, Mod...	16.7MByte/sec	ATA-3
<input type="checkbox"/> ULTRA DMA Mode 0	16.6MByte/sec	ATA-4
<input type="checkbox"/> ULTRA DMA Mode 1	25MByte/sec	ATA-4
<input type="checkbox"/> ULTRA DMA Mode 2	33MByte/sec	ATA-4
<input type="checkbox"/> ULTRA DMA Mode 3	44MByte/sec	ATA-5
<input type="checkbox"/> ULTRA DMA Mode 4	66MByte/sec	ATA-5
<input checked="" type="checkbox"/> ULTRA DMA Mode 5	100MByte/sec	ATA-6
<input type="checkbox"/> ULTRA DMA Mode 6	133MByte/sec	ATA-7

Range Section: This section contains a "Range" label and a "Decode Range" section. The "Decode Range" section has two dropdown menus: "From" (set to "Buffer Head") and "To" (set to "Buffer Tail").

At the bottom of the dialog are three buttons: "Default", "OK", and "Cancel".

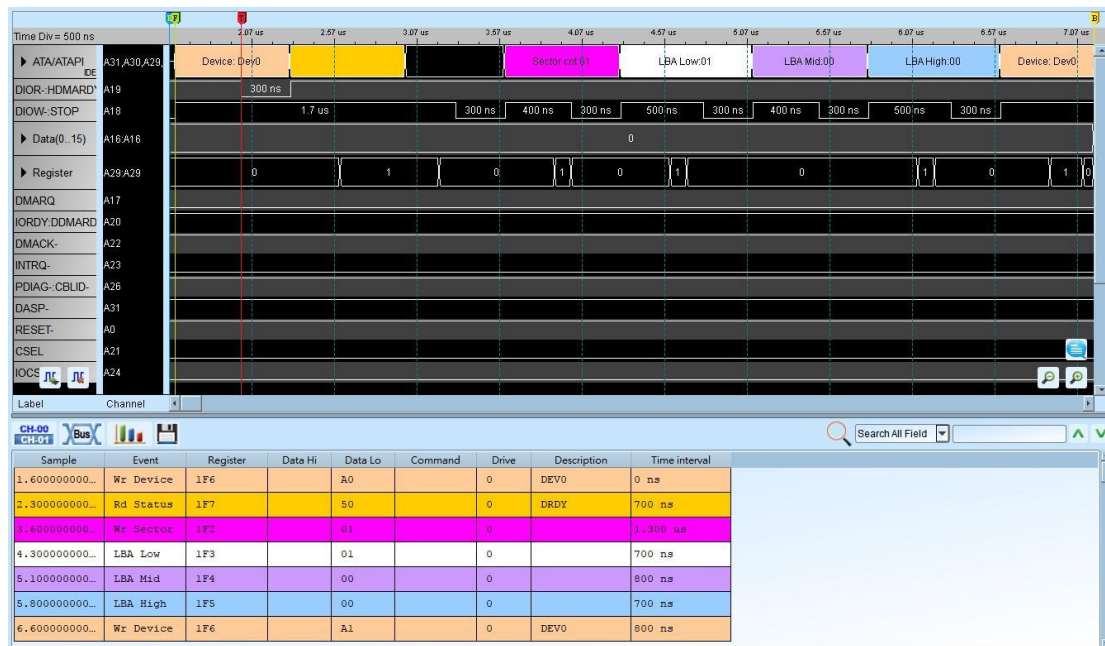
Channel: Set channel number for General, Register, and Data Bus.

Transferring Mode: Select the target system.

Analysis Report: Filter the data in the Report Window.

Result

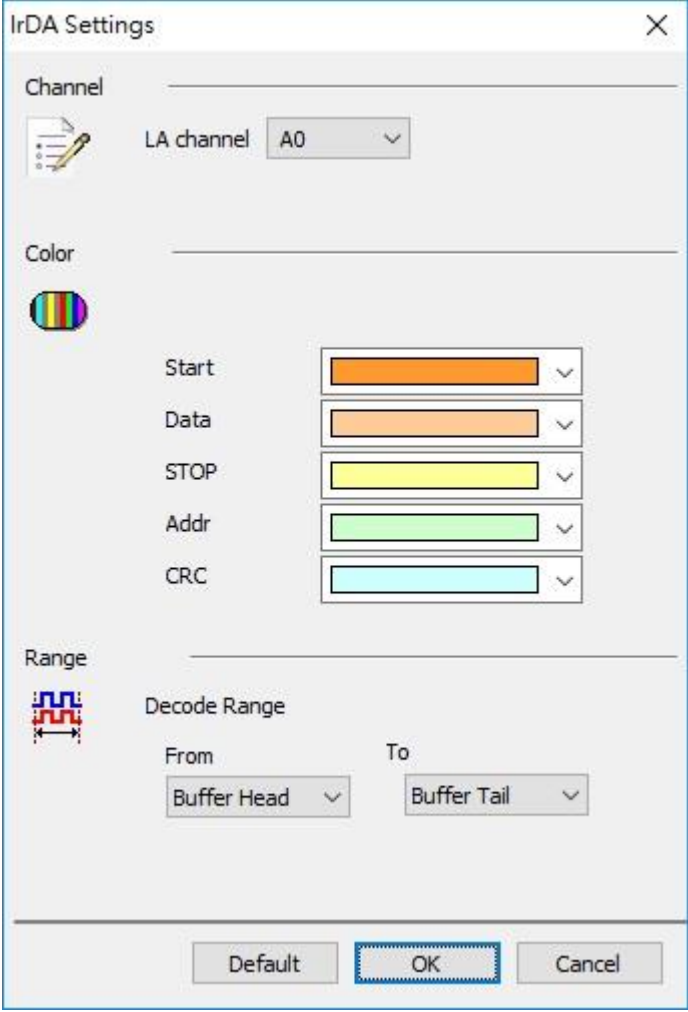
Click **OK** to run the IDE decode and see the result on the Waveform Window below.



IrDA

The Infrared Data Association (IrDA) was formed in 1993. The IrDA is point to point user model for a wide range of appliances and devices.

Settings



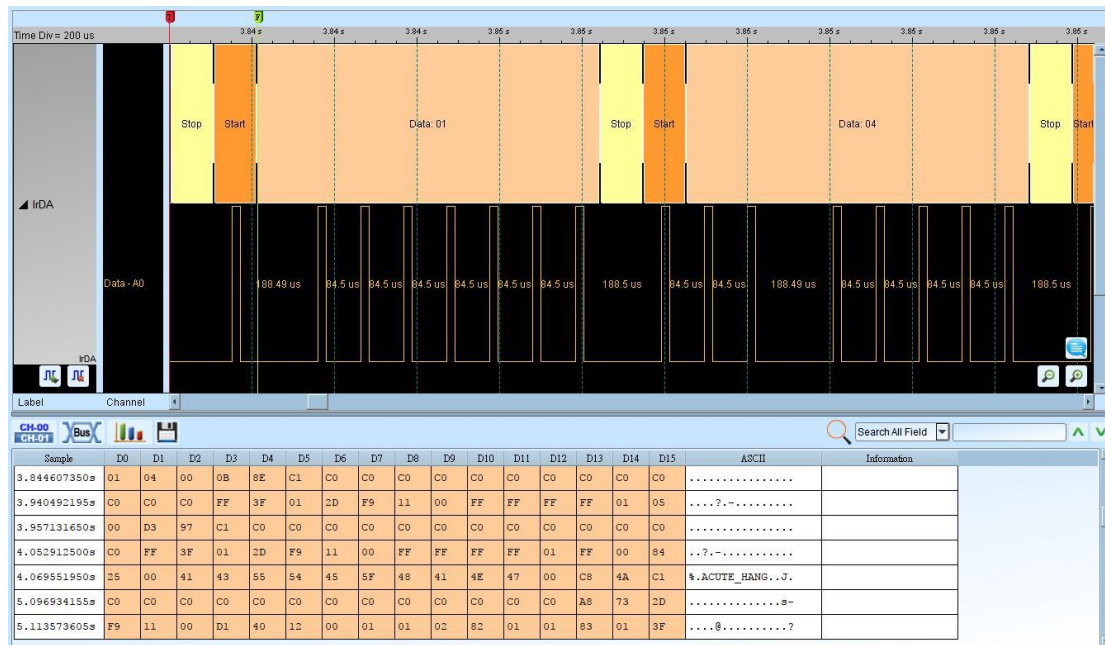
The image shows a software dialog box titled "IrDA Settings". It is organized into three main sections: "Channel", "Color", and "Range".

- Channel:** Features a "Channel" label and a "LA channel" dropdown menu currently set to "A0".
- Color:** Includes a color wheel icon and five color selection boxes with dropdown arrows:
 - Start: Orange
 - Data: Light Orange
 - STOP: Yellow
 - Addr: Light Green
 - CRC: Light Blue
- Range:** Includes a waveform icon and a "Decode Range" section with "From" and "To" dropdown menus, both set to "Buffer Head" and "Buffer Tail" respectively.

At the bottom of the dialog are three buttons: "Default", "OK" (which is highlighted with a blue border), and "Cancel".

Channel: Show the selected channel.

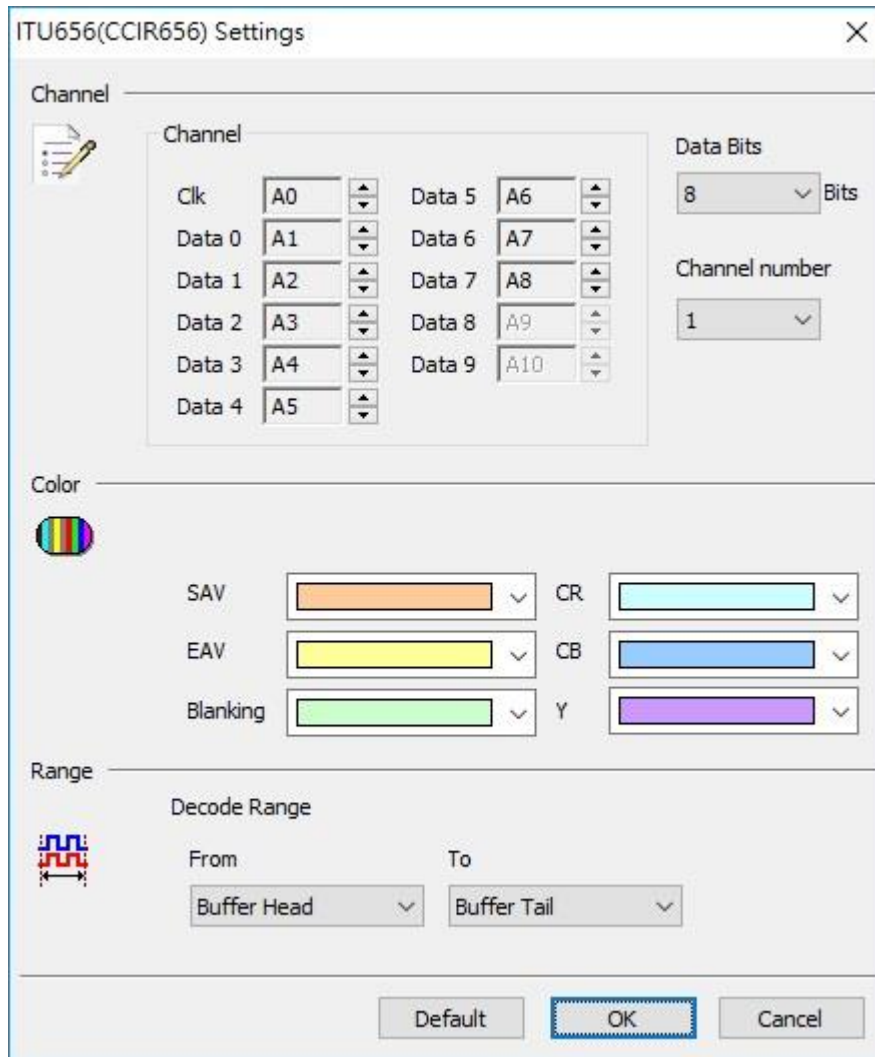
Result



ITU656 (CCIR656)

ITU656 describes a simple digital video protocol for streaming uncompressed PAL or NTSC Standard Definition TV (525 or 625 lines) signals. The protocol builds upon the 4:2:2 digital video encoding parameters defined in ITU-R Recommendation BT.601, which provides interlaced video data, streaming each field separately, and uses the YCbCr color space and a 13.5 MHz sampling frequency for pixels.

Settings



The dialog box is titled "ITU656(CCIR656) Settings" and contains three main sections: Channel, Color, and Range.

Channel Section: Includes a "Channel" icon (pencil and paper) and a table of channel settings. The table has two columns: "Data" and "Address". The "Data" column lists Clk, Data 0, Data 1, Data 2, Data 3, Data 4, Data 5, Data 6, Data 7, Data 8, and Data 9. The "Address" column lists A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, and A10. Each cell contains a dropdown menu with up and down arrows. To the right of the table are two dropdown menus: "Data Bits" (set to 8) and "Channel number" (set to 1).

Color Section: Includes a "Color" icon (rainbow bar) and six color selection boxes. The boxes are labeled SAV, EAV, Blanking, CR, CB, and Y. Each box contains a color swatch and a dropdown arrow.

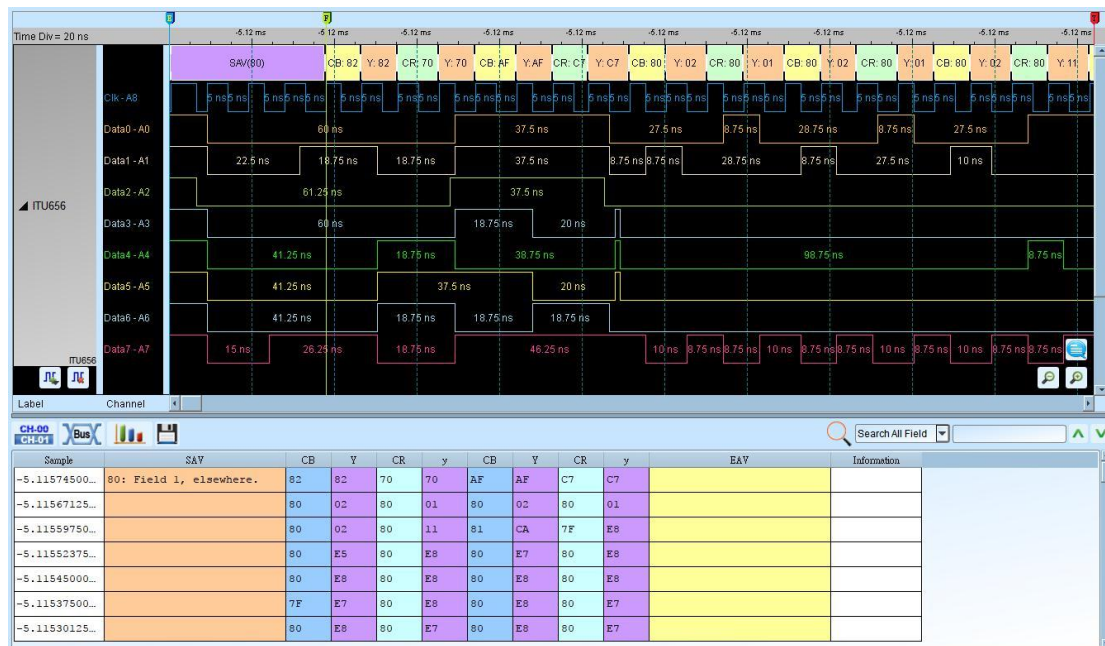
Range Section: Includes a "Range" icon (sine wave) and a "Decode Range" section. The "Decode Range" section has two dropdown menus: "From" (set to Buffer Head) and "To" (set to Buffer Tail).

At the bottom of the dialog are three buttons: "Default", "OK", and "Cancel".

Channel: Show the selected channel (Clk, Data 0 – Data 9).

Data Bits: Show the number of data bits.

Result

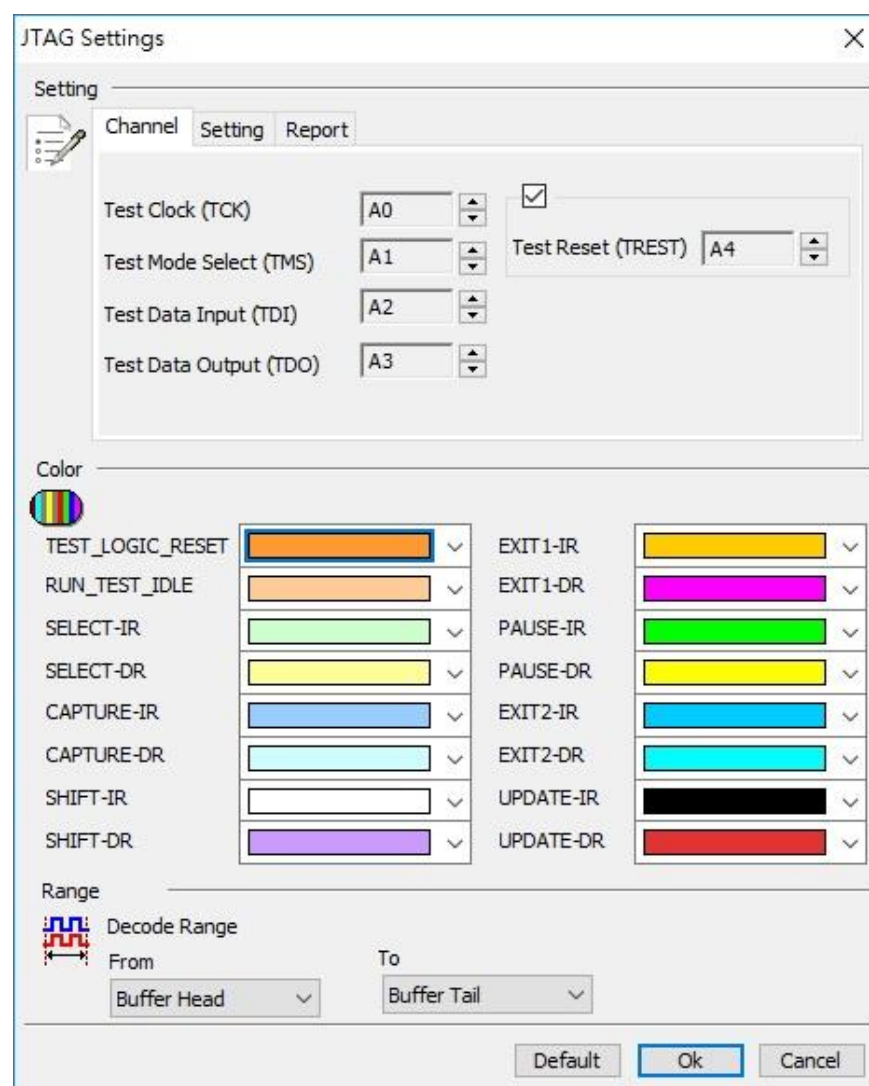


JTAG

Joint Test Action Group (JTAG) is the common name used for the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture for test access ports used for testing printed circuit boards using boundary scan.

A JTAG interface is a special four/five-pins interface added to a chip, designed so that multiple chips on a board can have their JTAG lines daisy-chained together if specific conditions are met, and a test probe need only connect to a single "JTAG port" to have access to all chips on a circuit board.

Settings



The JTAG Settings dialog box is divided into three tabs: Channel, Setting, and Report. The Setting tab is active, showing configuration options for JTAG signals. The 'Test Clock (TCK)' is set to A0, 'Test Mode Select (TMS)' to A1, 'Test Data Input (TDI)' to A2, and 'Test Data Output (TDO)' to A3. A checkbox for 'Test Reset (TREST)' is checked, with its pin set to A4. Below these settings is a 'Color' section with a color palette icon and two columns of color selection boxes for various JTAG signals. The 'Range' section at the bottom includes a 'Decode Range' icon and 'From' and 'To' dropdown menus, both currently set to 'Buffer Head' and 'Buffer Tail' respectively. At the bottom right are 'Default', 'Ok', and 'Cancel' buttons.

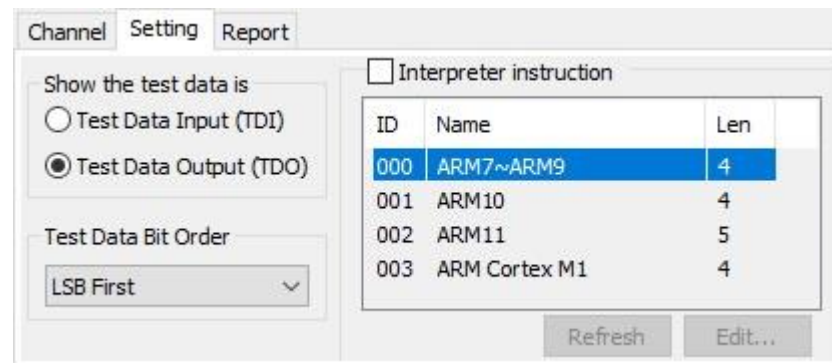
Signal	Color
TEST_LOGIC_RESET	Orange
RUN_TEST_IDLE	Light Orange
SELECT-IR	Light Green
SELECT-DR	Yellow
CAPTURE-IR	Blue
CAPTURE-DR	Light Blue
SHIFT-IR	White
SHIFT-DR	Purple
EXIT1-IR	Yellow
EXIT1-DR	Magenta
PAUSE-IR	Green
PAUSE-DR	Yellow
EXIT2-IR	Cyan
EXIT2-DR	Cyan
UPDATE-IR	Black
UPDATE-DR	Red

Settings: Includes Channel, Setting, and Report.

Channel: Set the channel number.

Show the test data is: The data is TDI or TDO.

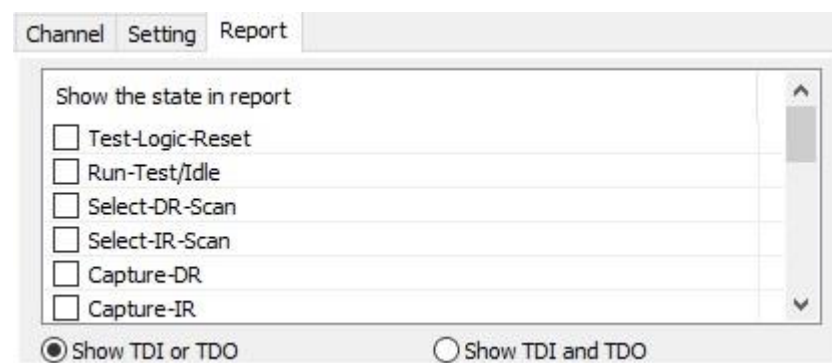
Test Data Bit Order: LSB First or MSB First.



Interpreter instruction: Check the Interpreter Instruction and you will see a list of commands. The JTAG decode will display its updated commands in the Instruction Register, which is the temporary memory buffer for the commands. Click Edit to edit the commands in the Interpreter Instructions; then click Refresh to update the commands in the Interpreter Instructions.

JTAG Instruction table (JtagInst.txt): This file is supported by the JTAG DLL and can be modified if needed. The JTAG Decode also supports the BSDL format. You can load the BSDL file in order to save time on editing commands. If you are interested in more details, please refer to the JTAG Instruction table Syntax Description in the end of the JTAG Decode chapter.

Report: You can filter the data you want to see on the Report Window.



Show TDI or/and TDO

Result



JTAG Instruction table Syntax Description (JtagInst.txt):

The numbers used in this file are hexadecimal.

##: is comment.

#ID: Command list number; the range is 00 - FF and , MUST be entered in order or will be seen as the end of commands.

#NAME: Command Name, 32 bytes most will be shown in the command list.

#LENGTH: Command length, unit in bits.

#CAPTURE: Command Capture Code, is stored in Instruction Register..

#INST: Command List, listed by Command Code and Command Name or will be seen as the end of commands..

#TRST: Enter 1 if TREST is needed or enter 0 or nothing if TREST is not needed.

#BSDL: Load the BSDL file. Use the BSDL file as step 1-6.

Example:#ID:00

#NAME:ARM7-ARM9

#LENGTH:4

#CAPTURE:1

#INST:0, EXTEST

#INST:2, SCAN_N

#INST:3, SAMPLE/PRELOAD

#INST:4, RESTART

#INST:5, CLAMP

#INST:7, HIGHZ

#INST:9, CLAMPZ

#INST:C, INTEST

#INST:E, IDCODE

#INST:F, BYPASS

#INST:

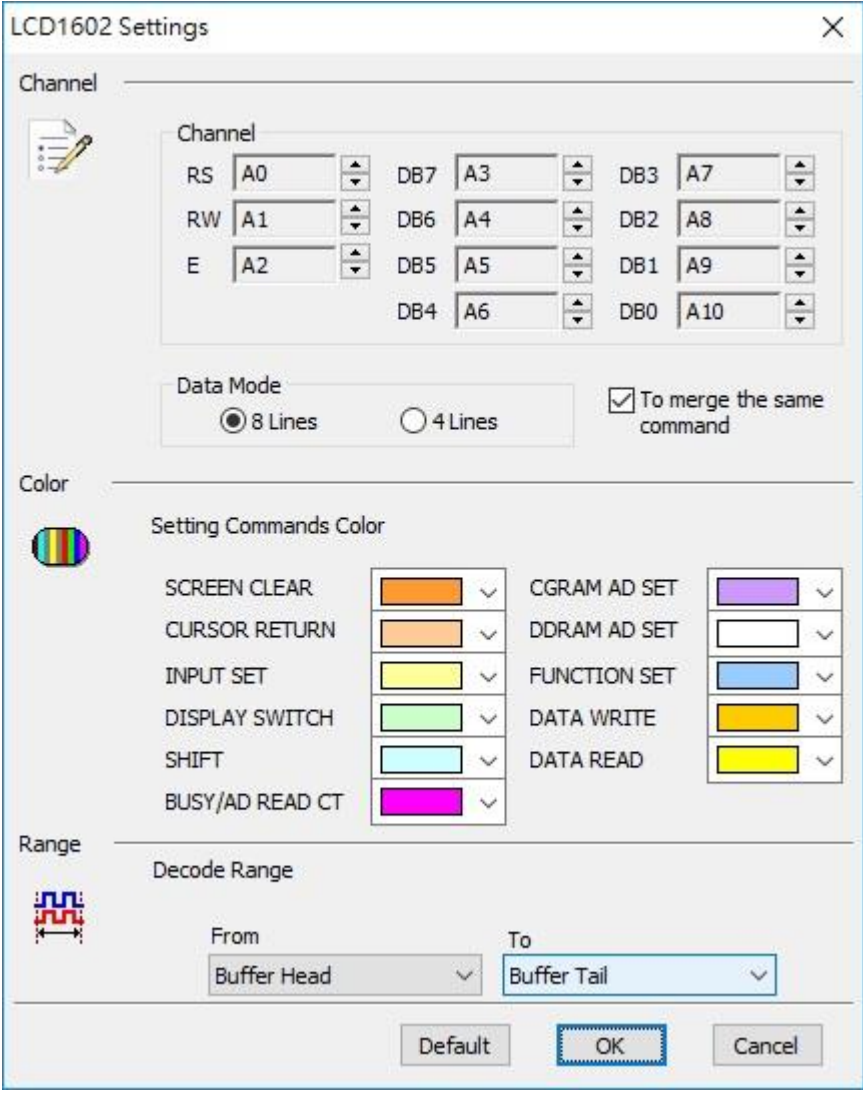
#ID:01

#BSDL:C:\3256at144_1532.bsd

LCD1602

The Liquid Crystal Display 1602 (LCD1602) bus has 11 data bits: Instruction/Data Register Select (RS), Read/Write Select (RW), Enable Select (E) and 8 bits or 4 bits Data Input/Output lines (DB0~DB7/DB0~DB3).

Settings



The LCD1602 Settings dialog box is divided into three main sections: Channel, Color, and Range.

Channel Section: This section allows users to assign specific channels to the RS, RW, E, and data lines (DB0-DB7). The RS, RW, and E lines are each assigned to a single channel (A0, A1, A2 respectively). The data lines (DB0-DB7) are assigned to channels A3 through A10. Below this, the Data Mode is set to 8 Lines (selected) or 4 Lines. A checkbox labeled "To merge the same command" is checked.

Color Section: This section allows users to assign colors to various LCD commands. The commands listed are SCREEN CLEAR, CURSOR RETURN, INPUT SET, DISPLAY SWITCH, SHIFT, BUSY/AD READ CT, CGRAM AD SET, DDRAM AD SET, FUNCTION SET, DATA WRITE, and DATA READ. Each command has a corresponding color selection box.

Range Section: This section allows users to set the Decode Range. The From field is set to Buffer Head and the To field is set to Buffer Tail.

At the bottom of the dialog are buttons for Default, OK, and Cancel.

Channel: Show the selected channels (RS: CH0, RW: CH1,..., DB0: CH10).

Data Mode: 8 lines or 4 lines.

To merge the same command: Merge data with its command.

Result

Click **OK** to run the LCD1602 decode and see the result on the Waveform Window below.



LIN

The Local Interconnect Network (LIN) bus (version 2.1) has two message types: Header and Response.

- (1) Header contains three data frames: Synchronization Break (Break), Synchronization Field (Sync) and Identifier Field (Identifier).
- (2) Response contains two data frames: Data Field (Data) and Checksum Field (Checksum). Checksum contains data and identifier (Enhanced mode), but version 1.3 or below (Classic mode) contains data only.

LIN bus has two states - Sleep mode and Active mode. While data is on the bus, all LIN nodes are in active state; but after a specified timeout, the nodes enter Sleep mode and will be released back to active state by a WAKEUP frame.

Settings

LIN Settings

Channel

Version

☒ LIN 2.1 ☐ LIN 2.0 ☐ LIN 1.2

Checksum mode

☒ Classic ☐ Enhanced

LA Channel A0 ☒ Show scale

Baud rate AUTO bps

Color

Wake-up

Break

Synch

Identifier

Data

Checksum

Range

Decode Range

From Buffer Head

To Buffer Tail

Default OK Cancel

Version: Select LIN version.

Checksum Mode: Select Classic: data only or Enhanced: data and identifier.

LA Channel: Show the selected channel (CH0 for LIN).

Show Scale: Show scale on the waveform.

Baud rate: Show the selected baud rate.

Result

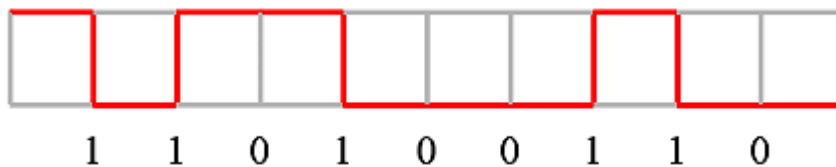
Click **OK** to run the Lin decode and see the result on the Waveform Window below.



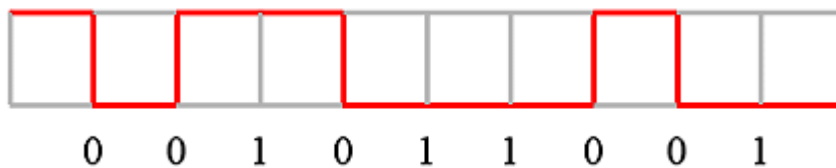
Line Decoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

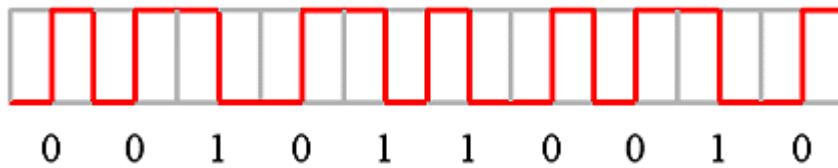


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.

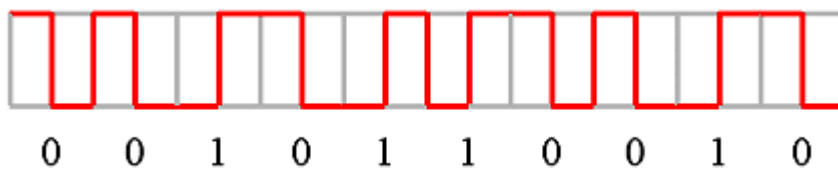


Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.



Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit's signal i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions which makes clock recovery and synchronization difficult. When

encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that together form a bit.



Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

Delay encoding is used primarily for encoding radio signals because the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



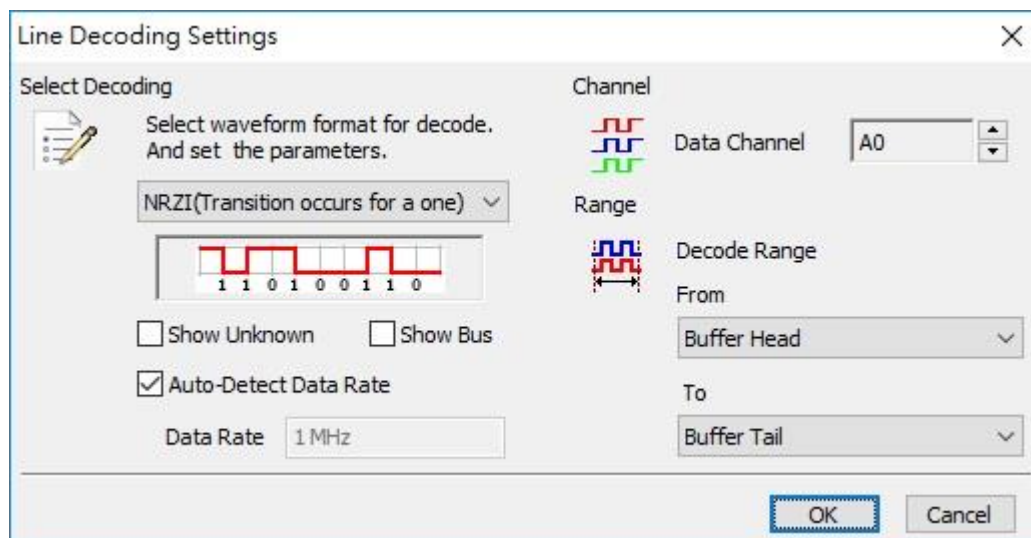
Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits

and synchronizing clock pulses which are output from the data separation circuit.

This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Decoding: Select the line code you want to decode.

Show Unknown: Display unknown data.

Show Bus: Display bus data.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate is not selected.

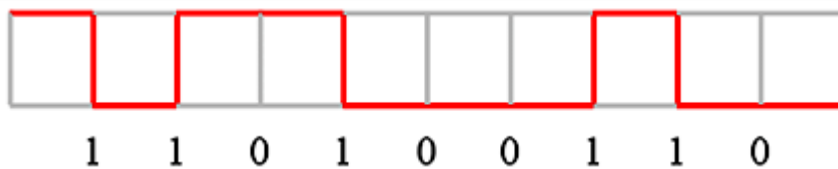
Channel: Show the selected channel (CH 0).

Range: Select the range within the waveform you want to decode.

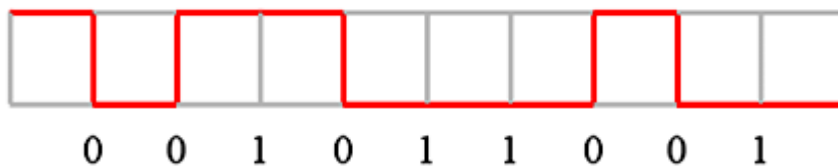
Line Encoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

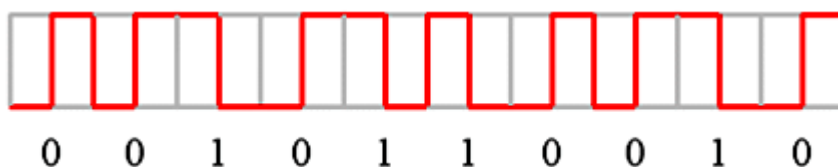


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.

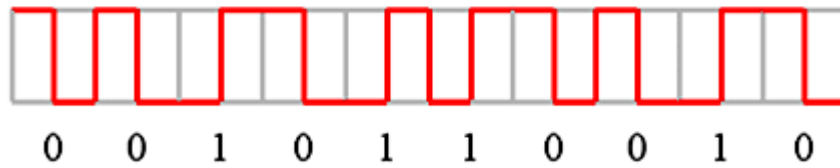


Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.



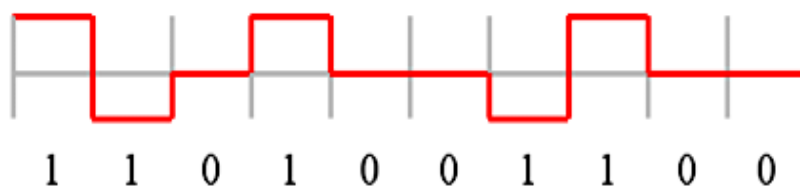
Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit, i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.

AMI (Alternate Mark Inversion): There are four modes:

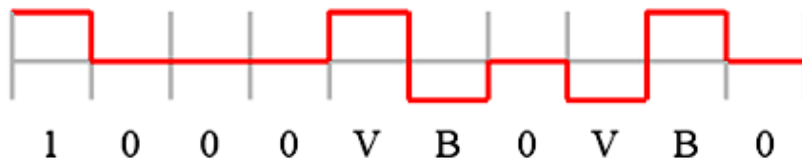
AMI (Standard): AMI (Alternate Mark Inversion) is a synchronous clock encoding technique that uses bipolar pulses to represent logical 1 value. It is therefore a three level system. A logical 0s is represented by no symbol, and a logical 1 is represented by alternating-polarity pulses.



AMI (B8ZS): Bipolar-8-Zero Substitution

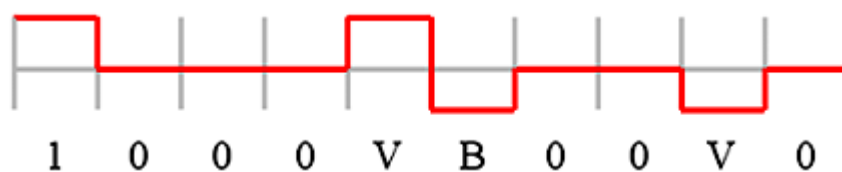
If 1 is +, 00000000 is represented to 000+-0-+

1 is -, 00000000 is represented to 000-+0+-



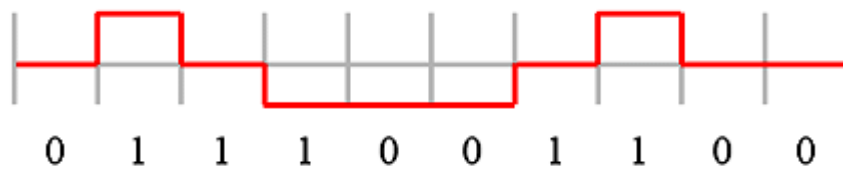
AMI (HDB3): High Density Bipolar 3

The HDB3 code is a bipolar signaling technique (i.e. relies on the transmission of both positive and negative pulses). It is based on Alternate Mark Inversion (AMI), but extends this by inserting violation codes whenever there is a run of 4 or more 0's. This and similar (more complex) codes have replaced AMI in modern distribution networks. The encoding rules follow those for AMI, except that sequences of four consecutive 0's are encoding using a special "violation" bit. This bit has the same polarity as the last 1-bit which was sent using the AMI encoding rule. The purpose of this is to prevent long runs of 0's in the data stream that may otherwise prevent a DPLL from tracking the center of each bit. Such a code is sometimes called a "run length limited" code, since it limits the runs of 0's that would otherwise be produced by AMI. One refinement is necessary, to prevent a dc voltage being introduced by excessive runs of zeros. This refinement is to encode any pattern of more than four bits as B00V, where B is a balancing pulse. The value of B is assigned as + or -, so as to make alternate "V"s of opposite polarity. The receiver removes all Violation pulses, but in addition a violation preceded by two zeros and a pulse is treated as the "B00V" pattern and both the violation and balancing pulse are removed from the received bit stream. This restores the original bit stream.

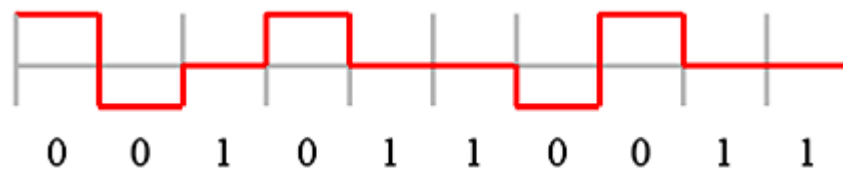


MLT-3: Multilevel Transmission 3: A 0 means no transition happens, a 1 is

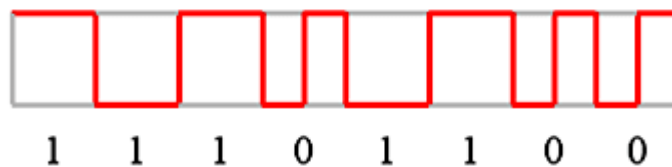
represented by a transition (0, +, 0, -).



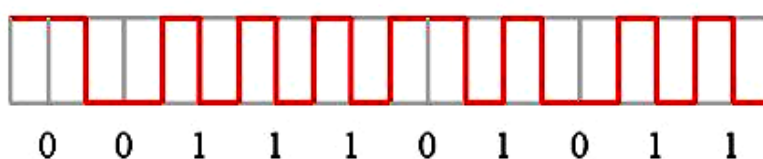
Pseudoternary: A 1 is always zero, a 0 is represented by a transition (+, -).



CMI (Coded Mark Inversion): A zero is sent a low to high [01] transition, while a one is sent as either a one [1] or zero [0] depending on the previous state. If the previous state was high the one is sent as a zero [0], if it was low the one is sent as a one [1].



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions that make clock recovery and synchronization difficult. When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that form a bit.



Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

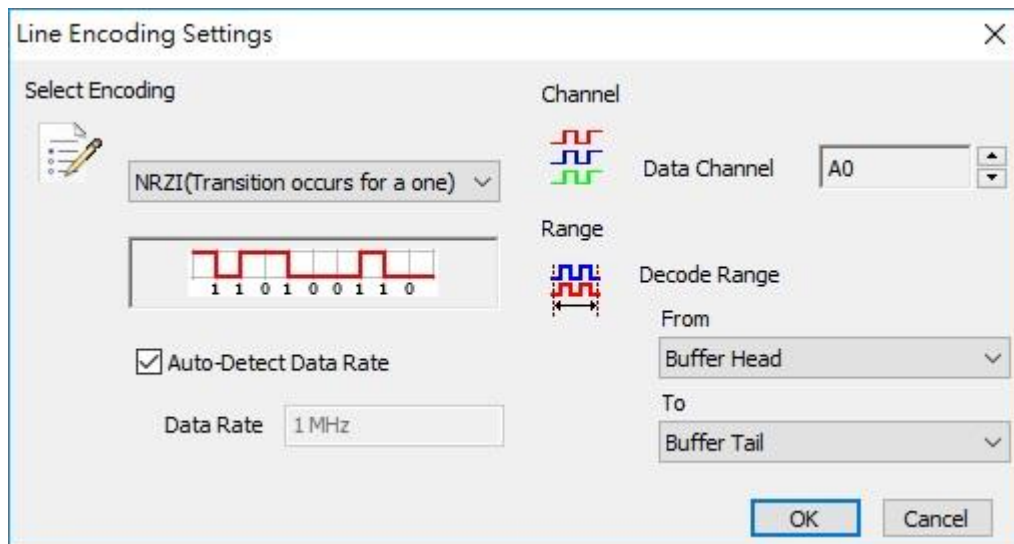
Delay encoding is used primarily for encoding radio signals because the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit. This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Encoding: Select the line code you want to encode.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate is not selected.

Channel: Show the selected channel (CH 0).

Range: Select the range within the waveforms you want to encode.

Low Pin Count (LPC)

The LPC bus, for the data transmissions, was developed by Intel to replace the ISA bus.

Settings

LPC Settings

Channel

LFRAME# A1 LAD[2] A4 LCLK A0

LAD[0] A2 LAD[3] A5 Data Edge Rising

LAD[1] A3

Show the field in report

- ☒ START
- ☒ CYCLETYP+DIR
- ☒ SIZE
- ☒ TAR
- ☒ ADDR

Color

START ADDR

CYCLETYP+DIR DATA

CHANNEL SYNC

TAR IDSEL

SIZE/MSIZE STOP

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Channel: Show the selected channels.

LFRAME#: Frame indicator.

LAD[0-3]: Data bits.

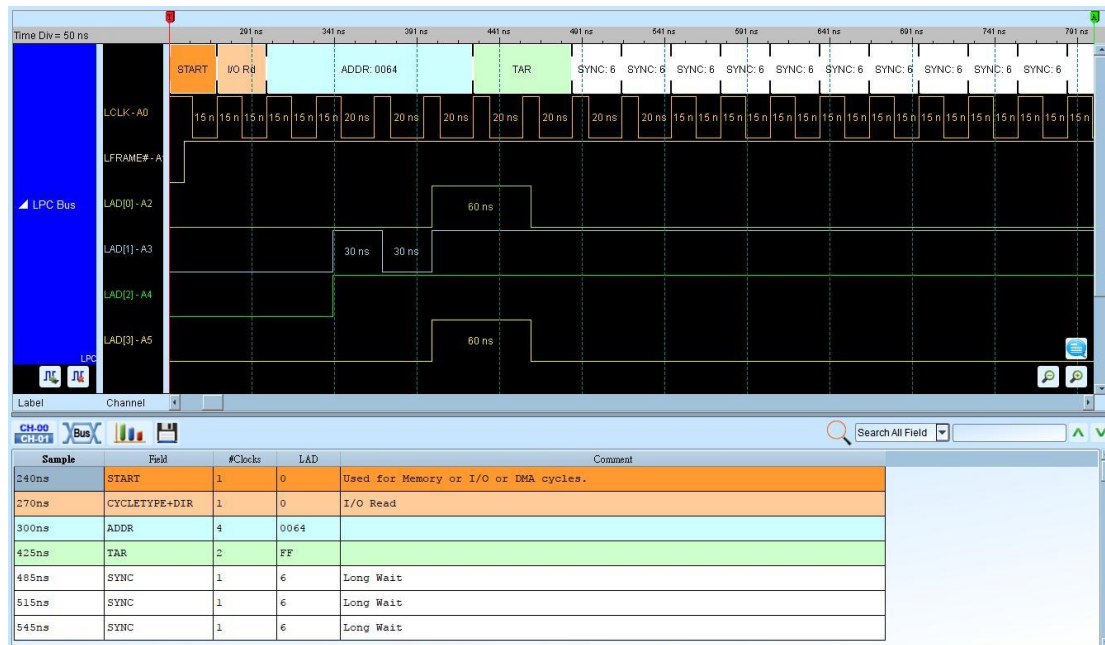
LCLK: Clock.

Filter the data in the report window: You can filter the data in the Report Window.

Result

Click **OK** to run the LPC decode and see the result on the Waveform Window below.

I/O Read Cycle.

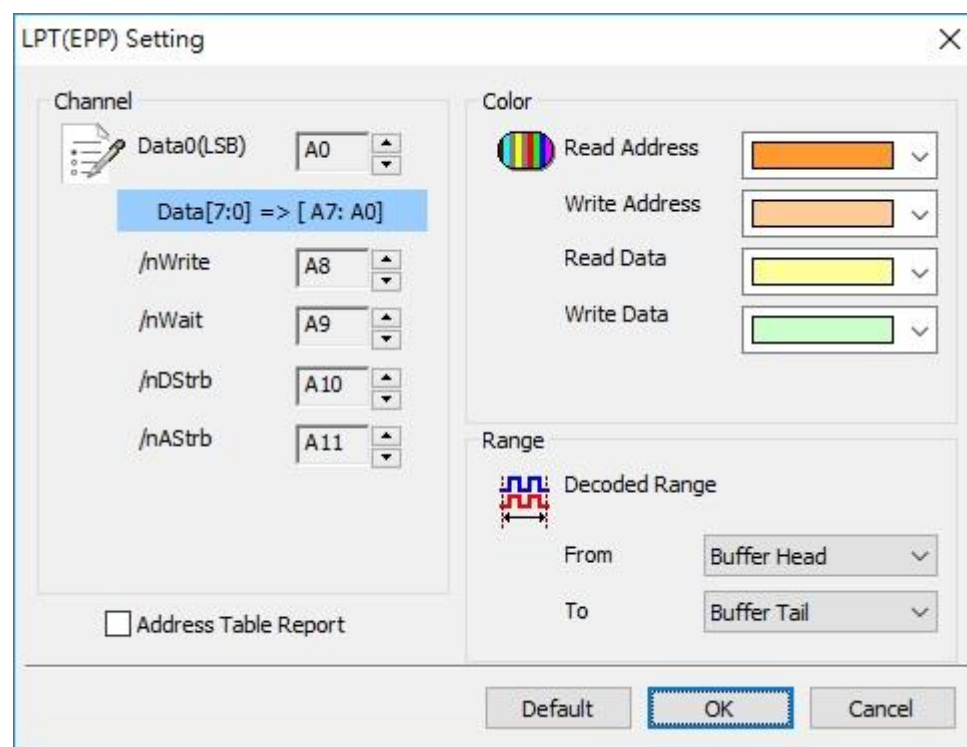


Line Printer Terminal Port (LPT)

LPT is a universal parallel interface that use in PC since 1980's. It was primarily designed to operate a line printer, but could also be used to adapt other peripherals.

This decode only support EPP Mode.

Settings



Data0(LSB): There are 8 data channel. Only set Data0(LSB) here, other channel will be set automatically.

/nWrite: Indicates the direction of transfer.

/nWait: To acknowledge that a transfer has finished.

/nDStrb: Indicates the data cycle.

/nAStrb: Indicates the address cycle.

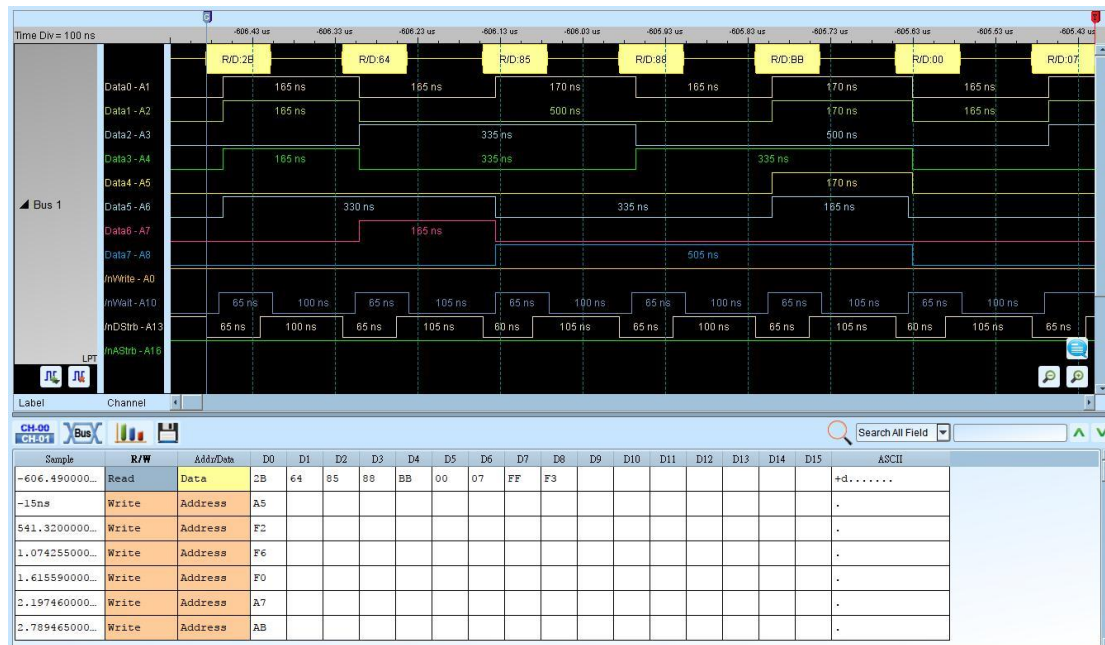
/nInit: Indicates a termination cycle in order to return the interface to the

Compatibility mode. User can option to use this channel or not.

/nIntr: This is an interrupt signal. User can option to use this channel or not.

Result

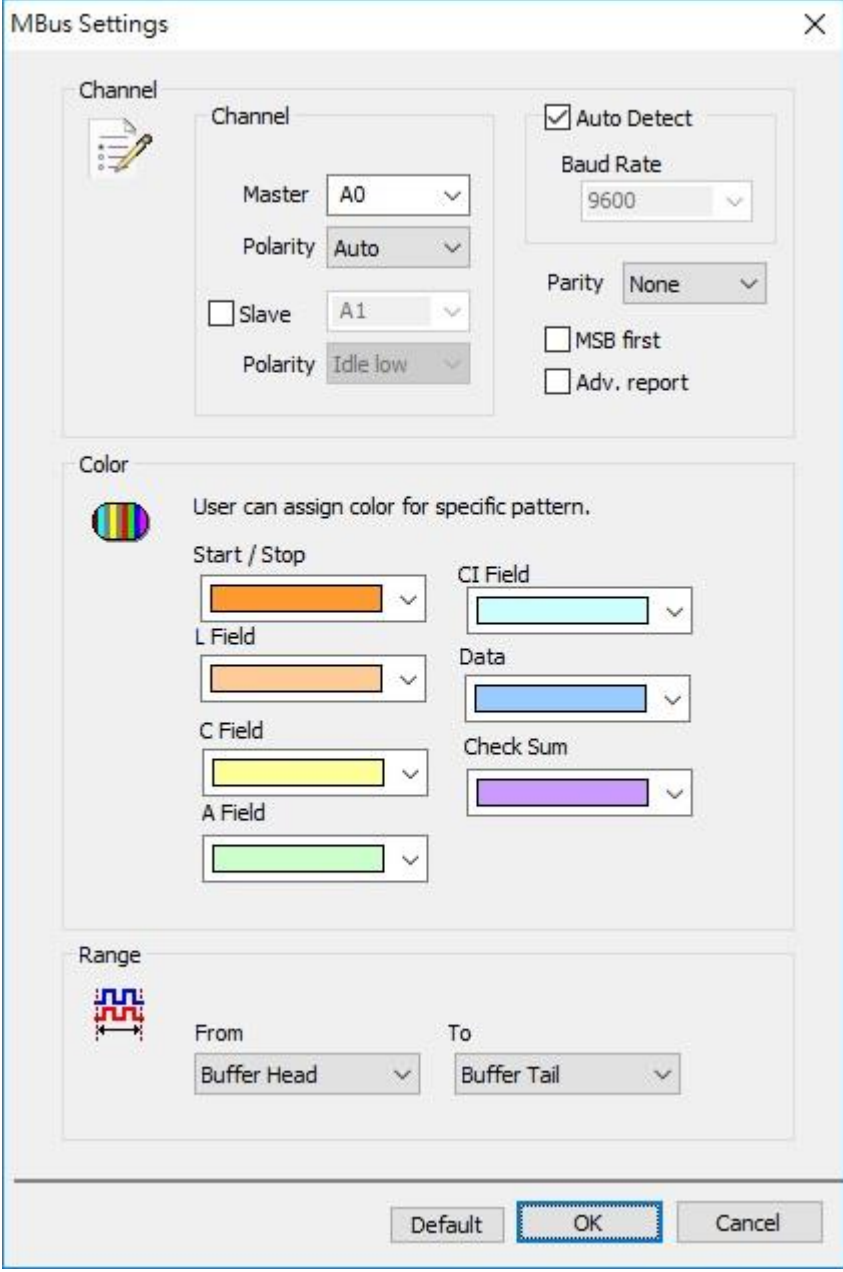
Click OK to run the LPT Decode and see result on the Waveform Windows below.



M-Bus

M-Bus (Meter-Bus) is for remote reading of heat meters and other types of consumption meters.

Settings



The M-Bus Settings dialog box is divided into three main sections: Channel, Color, and Range. The Channel section includes settings for Master/Slave channels, Polarity, Auto Detect, Baud Rate, Parity, MSB first, and Adv. report. The Color section allows users to assign colors for specific patterns, including Start / Stop, L Field, C Field, A Field, CI Field, Data, and Check Sum. The Range section allows users to set the range of the signal, from Buffer Head to Buffer Tail. The dialog box has a close button (X) in the top right corner and buttons for Default, OK, and Cancel at the bottom.

Channel

Channel

Master: A0

Polarity: Auto

☐ Slave: A1

Polarity: Idle low

☒ Auto Detect

Baud Rate: 9600

Parity: None

☐ MSB first

☐ Adv. report

Color

User can assign color for specific pattern.

Start / Stop: [Orange]

L Field: [Orange]

C Field: [Yellow]

A Field: [Green]

CI Field: [Cyan]

Data: [Blue]

Check Sum: [Purple]

Range

From: Buffer Head

To: Buffer Tail

Default OK Cancel

Channel: Set the channel of the signal and Polarity.

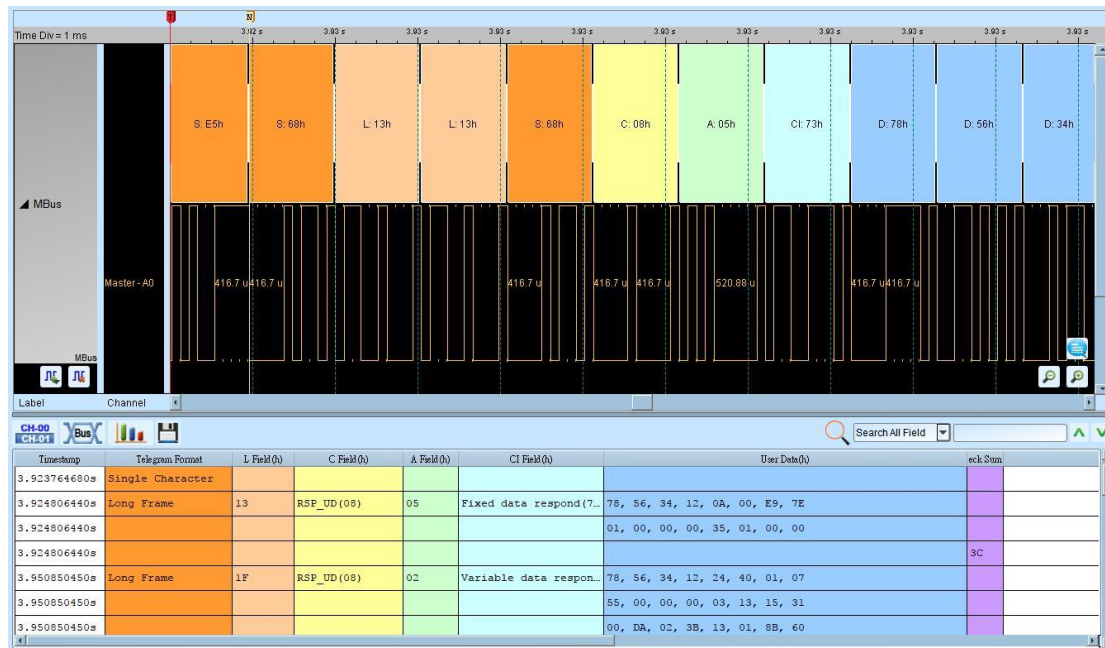
Baud rate: Set the specific data rate or auto detection.

Parity: Error detection.

MSB first: Set MSB format.

Adv. Report: Advanced report.

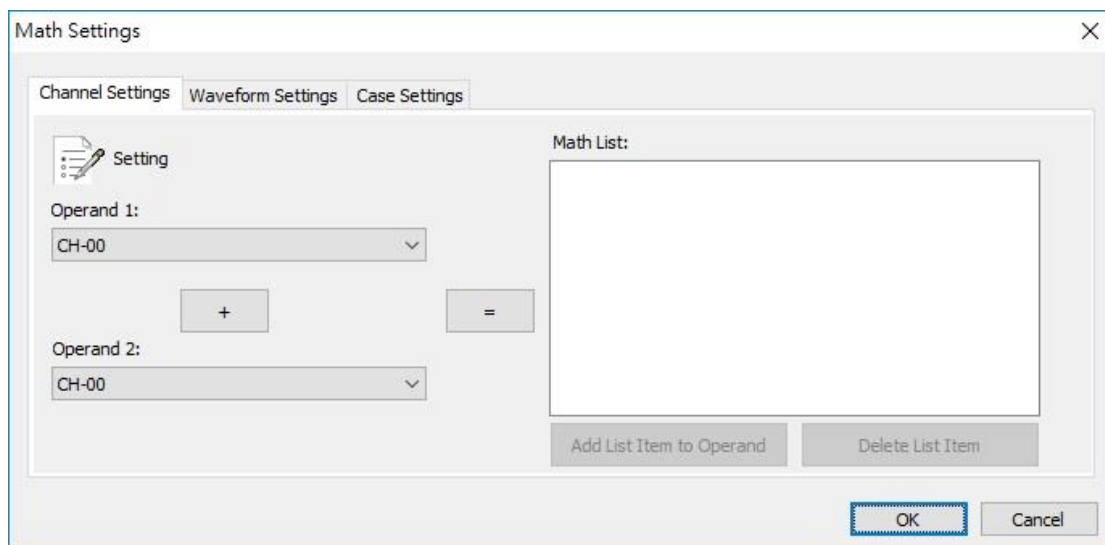
Result



Math

Math is used to conduct addition, subtraction, multiplication, division, AND, XOR, OR, NAND, NOR, XNOR operation for the channel or combined channels.

Settings



Operand: Select the channel(s) in the waveform window.

“+”: Select “+”, “-”, “X”, “/”, “AND”, “XOR”, “OR”, “NAND”, “NOR”, “XNOR” operator.

“=”: Add operation type.

Add List Item to Operand: Add operation type to operand.

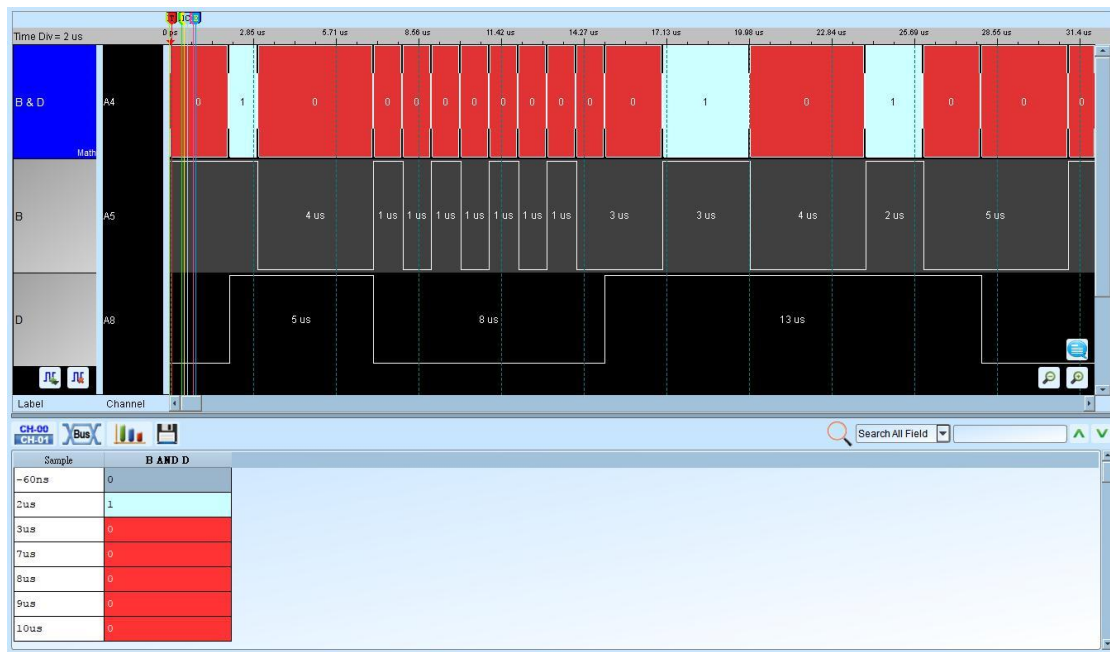
Delete List Item: Delete operation type from the list.

Color: Set the colors for the data bits.

Range: Select the range within the waveform you want to decode.

Case Settings: Select condition and frame color.

Result

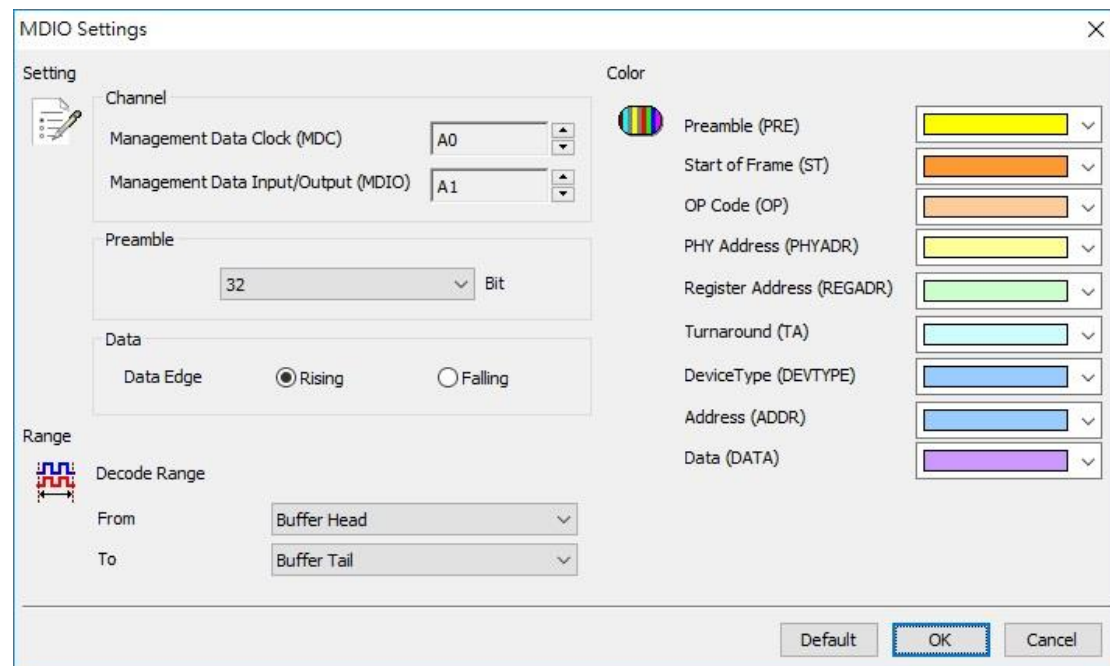


Note: When the Math settings are finished, the settings will always be saved as an independent text file named as AqMath.txt, different from the waveform file, at work directory unless other name assigned. If you need the specific Math settings, please save it, so you can reload the settings next time you open the specific waveform file.

MDIO

MDIO, also known as Serial Management Interface (SMI), is a serial bus defined for the Ethernet IEEE 802.3 specification for Media Independent Interface, or MII.

Settings



The MDIO Settings dialog box is divided into two main sections: 'Setting' and 'Color'.

Setting Section:

- Channel:** Includes 'Management Data Clock (MDC)' set to 'A0' and 'Management Data Input/Output (MDIO)' set to 'A1'.
- Preamble:** A dropdown menu is set to '32' with the unit 'Bit'.
- Data:** Includes a 'Data Edge' section with radio buttons for 'Rising' (selected) and 'Falling'.
- Range:** Includes a 'Decode Range' section with 'From' set to 'Buffer Head' and 'To' set to 'Buffer Tail'.

Color Section:

- A color palette icon is shown next to the list of fields.
- Fields and their assigned colors: Preamble (PRE) - Yellow, Start of Frame (ST) - Orange, OP Code (OP) - Light Orange, PHY Address (PHYADR) - Yellow, Register Address (REGADR) - Light Green, Turnaround (TA) - Light Blue, DeviceType (DEVTYPE) - Blue, Address (ADDR) - Blue, Data (DATA) - Purple.

Buttons: 'Default', 'OK' (highlighted with a dashed border), and 'Cancel'.

MDC: Clock.

MDIO: Data Input / Output.

Preamble: Set the MDIO preamble width, 32 bit default.

Data Edge: Set the MDC Rising/Falling edge to latch the data field, Rising Edge default.

Result

Click **OK** to run the MDIO decode and see the result on the Waveform Window below.



MHL-CBUS

Mobile High-definition Link (MHL) is an HD audio and video interface, Control Bus (CBUS) is used to control it.

Settings

CBUS Settings

Channel

Channel

CBUS A0

Range

Decode Range

From

Buffer Head

To

Buffer Tail

Color

SYNC

HEADER

cPacket

dPacket

CMD / DATA

PARITY

ACK

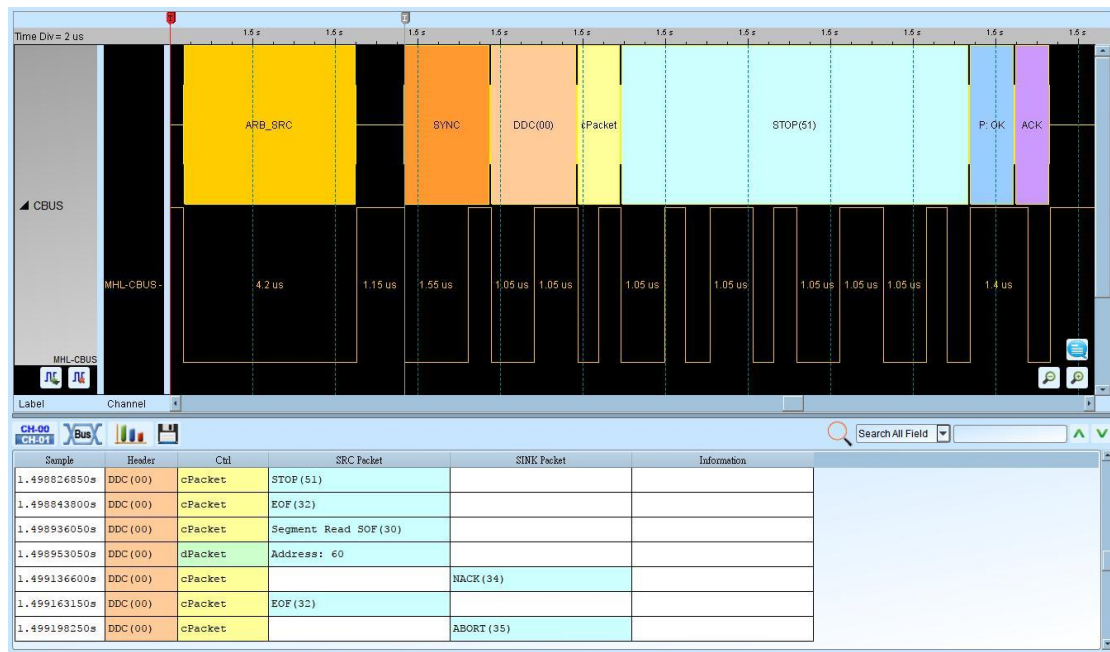
Arbitration

Default OK Cancel

LA Channel: Show the selected channel (CH0).

Result

Click OK to run the MHL-CBUS Decode and see result on the Waveform Window below.



MII/RMII

MII/RMII (Media Independent Interface/Reduced Media Independent Interface) is a protocol formulated by 802.3u that applied to Fast Ethernet, connecting MAC of Data Link Layer and PHY layer. Its clock frequency is either 25MHz or 2.5MHz (Ethernet); they are TX_CLK and RX_CLK. TX [0:3], RX [0:3] are 4-bit-width bus and TX_EN, RX_EN enable the IN/OUT; TX_ER, RX_ER can detect the errors on the bus; RX_DV inform bus the data received is valid or not; COL can detect the collision on the bus. **Serial Management Interface (SMI), also known as MDIO, is also an important part of MII.**

Settings

MII / RMII / GMII / RGMII Settings

Setting

Protocols

☐ MII ☐ RMII ☐ Only CLK and DATA pins used (MII)

☐ GMII ☐ RGMII ☐ Only CLK and DATA pins used (GMII)

Mode

☒ Transmit (Tx) ☐ Receive (Rx) ☐ Duplex (Tx+Rx)

Channel

The data source from DSO - Differential

Transmit (Tx)

TD+ DSO 1

TD- DSO 2

TX_D1 A2

TX_D2 A3

TX_D3 A4

TX_D4 A8

TX_D5 A9

TX_D6 A10

TX_D7 A11

TX_EN A5

TX_ER A6

TX_COL A7

Receive (Rx)

RD+ DSO 1

RD- DSO 2

RX_D1 A2

RX_D2 A3

RX_D3 A4

RX_D4 A7

RX_D5 A8

RX_D6 A9

RX_D7 A10

RX_DV A5

RX_ER A6

Data

Data Edge

☒ Rising ☐ Falling

Report

Data Columns

☒ 8 columns ☐ 16 columns

☒ Decode Ethernet Packet (MAC)

Color

Data

Error

Collision

Idle

Carrier Extend / False Carrier indication / Status

Preamble / SFD

Range

Decode Range

From Buffer Head To Buffer Tail

Default OK Cancel

MII / RMII: Select the MII / RMII bus decode

GMII / RGMII: Select the GMII / RGMII bus decode

Only CLK and Data pins used(M/G): Select MII / GMII the CLK and Data pins only.

Transmit (Tx): Select TX mode

Receive (Rx): Select Rx mode

Duplex (Tx+Rx) : Select duplex mode

Channel: Set the channel number.

Rising: Select rising edge to latch data

Falling: Select falling edge to latch data

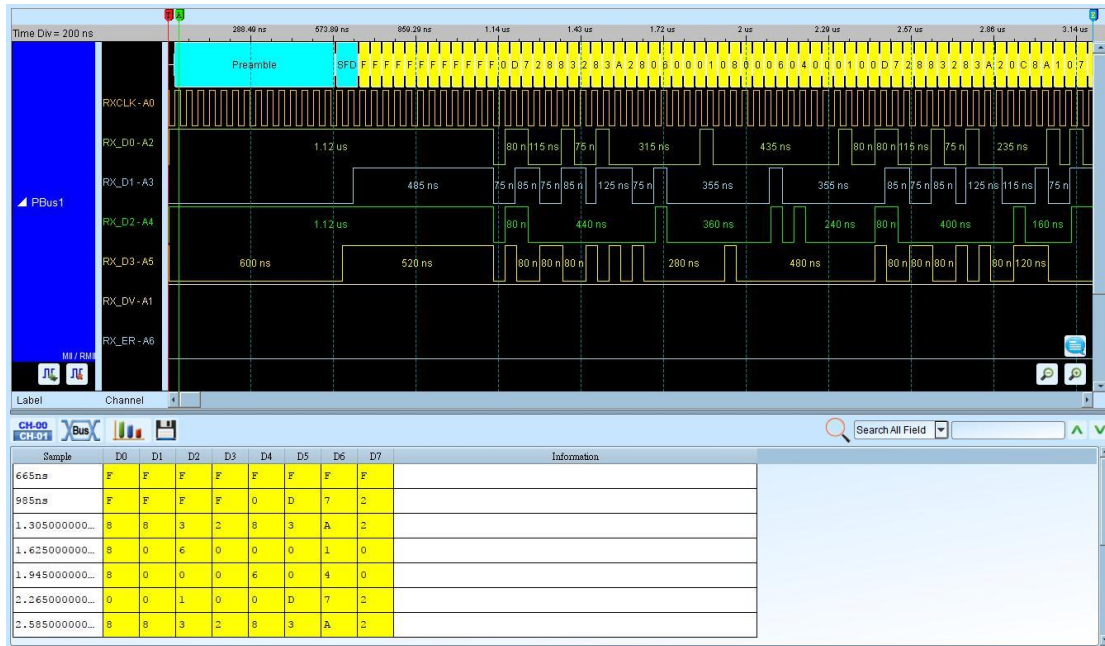
8 columns: show 8 columns data field in the report window

16 columns: show 16 columns data field in the report window

Result

Click **OK** to run the MII/RMII decode and see the result on the Waveform Window below.

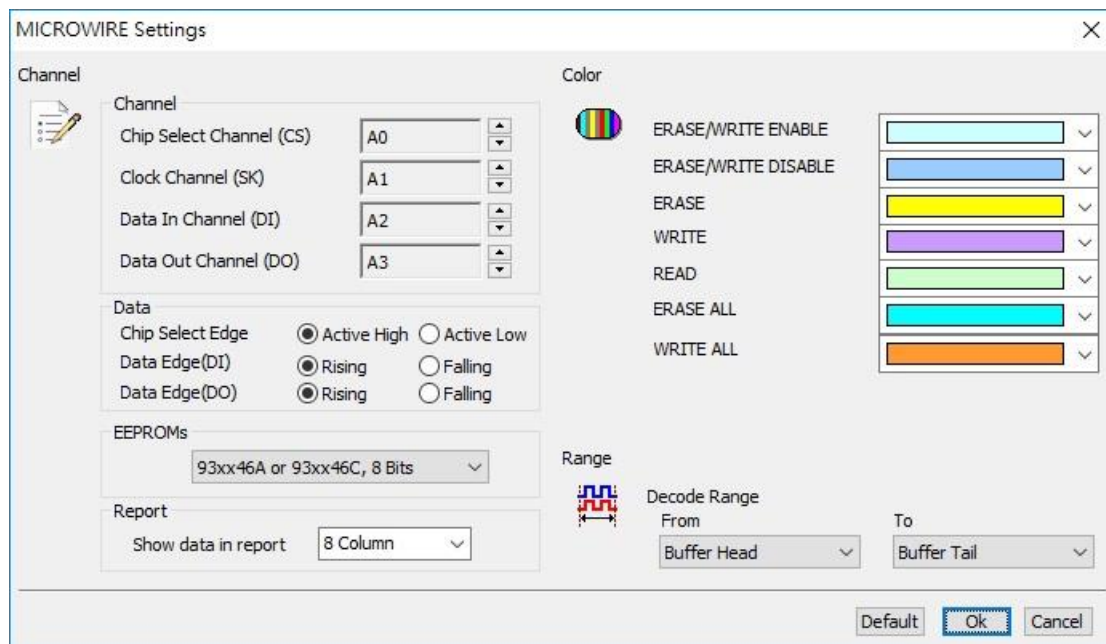
MII



Microwire

The Microwire bus has four data bits: Chip Select (CS), Serial Clock (SK), Data Input (DI), and Data Output (DO).

Settings



The MICROWIRE Settings dialog box is divided into several sections. The 'Channel' section on the left contains four dropdown menus for 'Chip Select Channel (CS)', 'Clock Channel (SK)', 'Data In Channel (DI)', and 'Data Out Channel (DO)', all set to A0, A1, A2, and A3 respectively. Below this is the 'Data' section with three rows of radio buttons: 'Chip Select Edge' (Active High selected), 'Data Edge (DI)' (Rising selected), and 'Data Edge (DO)' (Rising selected). The 'EEPROMs' section has a dropdown menu set to '93xx46A or 93xx46C, 8 Bits'. The 'Report' section has a dropdown menu set to '8 Column'. The 'Color' section on the right lists seven operations with corresponding color swatches: ERASE/WRITE ENABLE (light blue), ERASE/WRITE DISABLE (blue), ERASE (yellow), WRITE (purple), READ (light green), ERASE ALL (cyan), and WRITE ALL (orange). The 'Range' section at the bottom right has a 'Decode Range' section with 'From' and 'To' dropdowns set to 'Buffer Head' and 'Buffer Tail'. At the bottom are 'Default', 'Ok', and 'Cancel' buttons.

Channel: Show the selected channels.

Chip Select Edge: Active Low or Active High.

Data Edge: Rising or Falling.

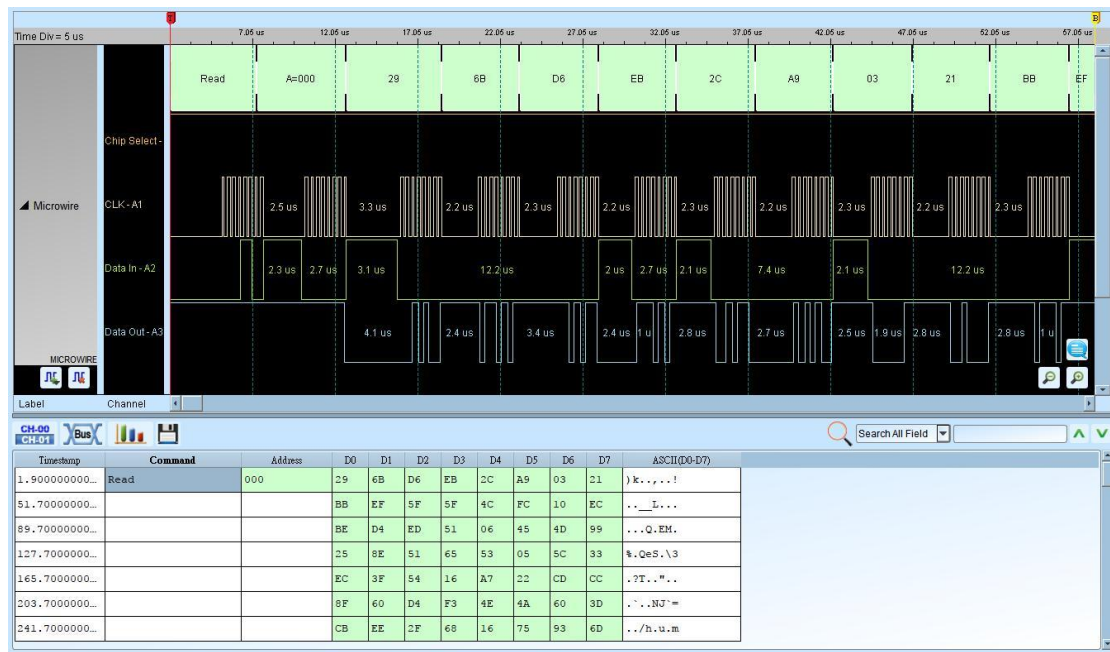
EEPROMs: Select EEPROMs.

Report: Show data in report.

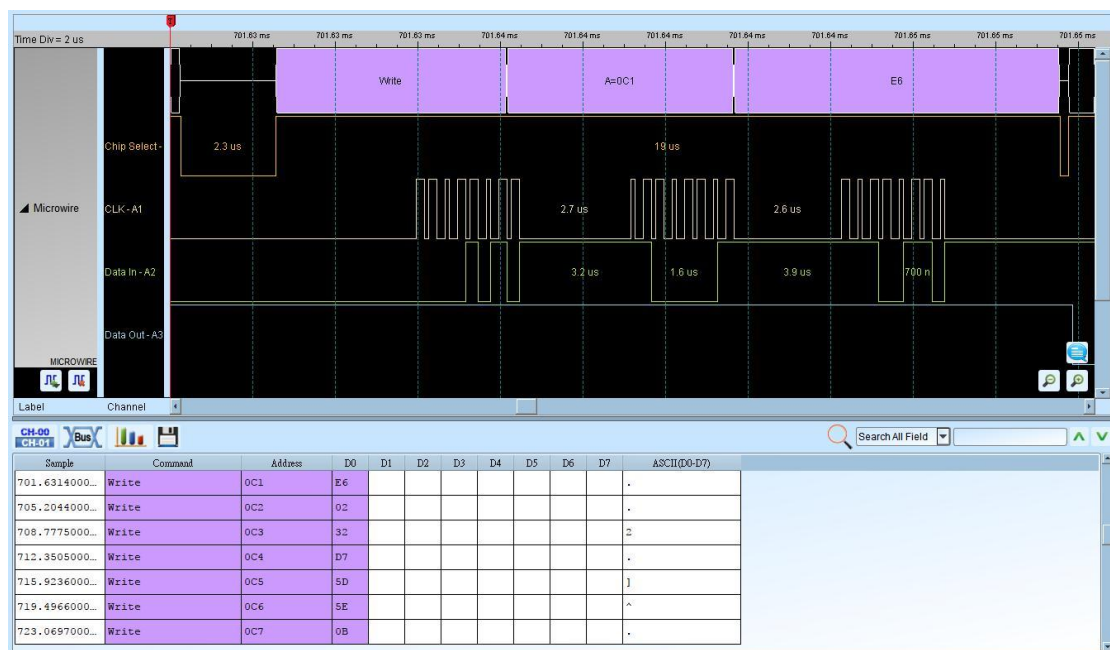
Result

Click **OK** to run the Microwire decode and see the result on the Waveform Window below.

Read



Write



MIPI DSI

MIPI Display Serial Interface (DSI) designed by MIPI alliance for the protocols between a host processor and peripheral devices using a D-PHY physical interface. The operation mode includes High Speed Mode and Low Power Mode (LPM).

Settings

MIPI DSI Settings

Channel

LP Mode Channel

Dp A0

Dn A1

HS Mode Channel

Data Lane 1

Clock + A2

D0+ A3

D1+ A4

D2+ A5

D3+ A6

Advanced Decode

Show DCS Command

Always goes to HS Mode

Initial Bus Direction Master -> Slave

Color

Start of Transmission

Transmission Mode

Escape Mode Action

Data Identifier

Word Count

Data Frame

End of Transmission

DCS Command

Range

Decode Range

From Buffer Head

To Buffer Tail

Default OK Cancel

Dp, Dn: DSI-LP signal lines

Data Lane: DSI-HS mode Data Lane number

Clock+, D0+, D1+, D2+, D3+: DSI-HS signal lines

Advanced Decode: Enable DSI format decode and display.

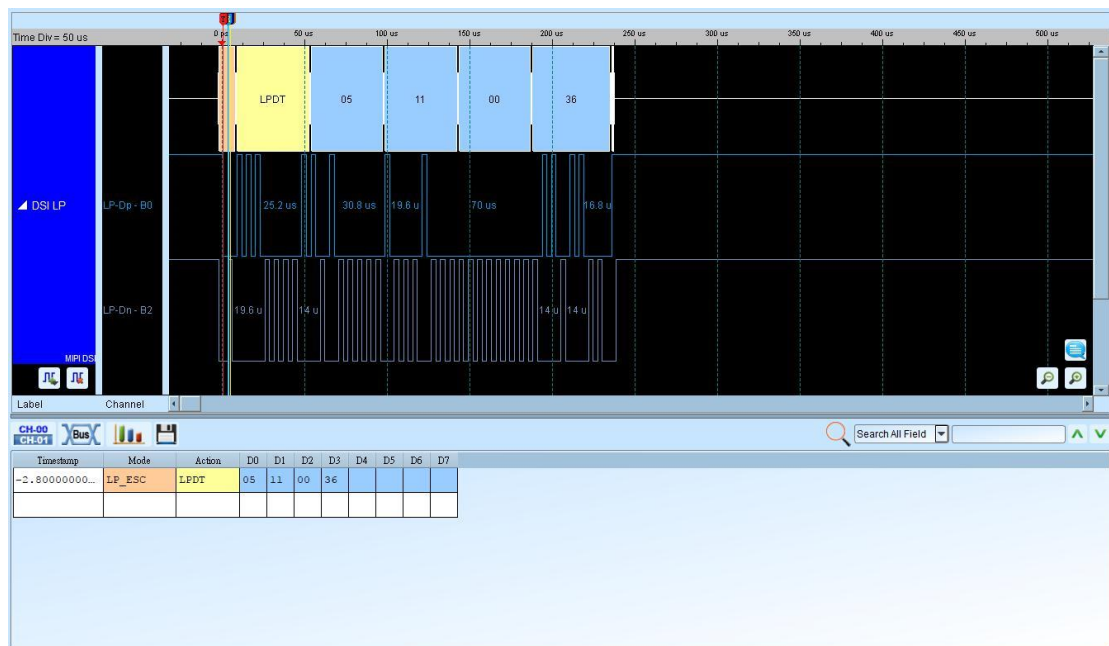
Show DCS Command: Enable DCS Command decode and display.

Always goes to HS Mode: Ignore the Dp and Dn status and decode all the data frame in HS mode

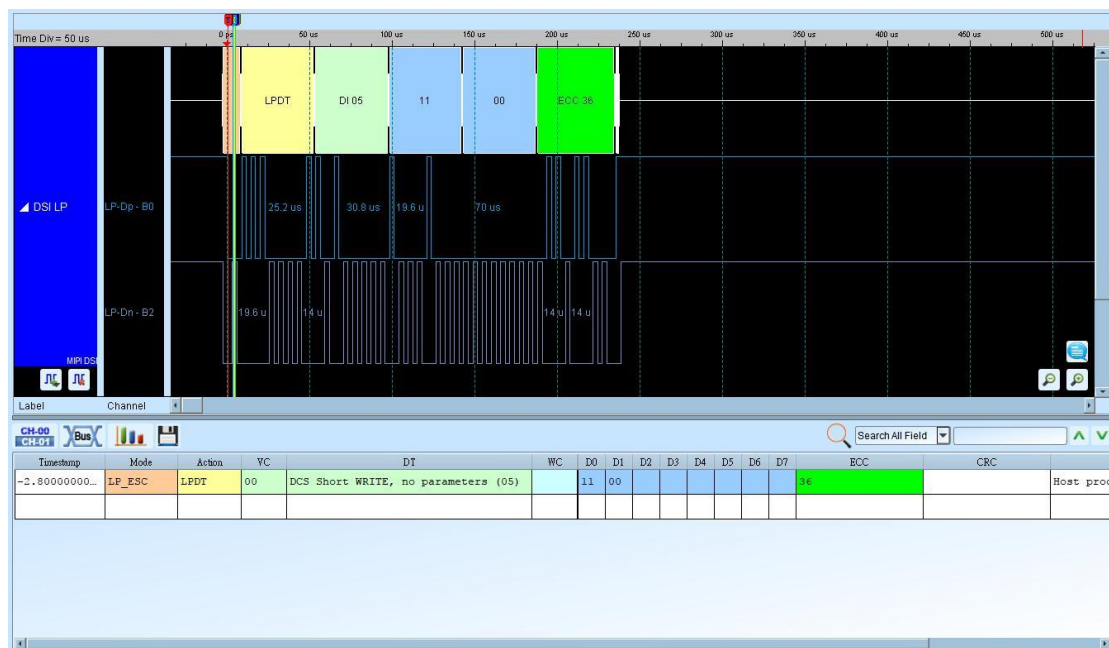
Initial Bus Direction: Select the Initial direction of the bus transmission.

Result

Advanced Decode Disabled:



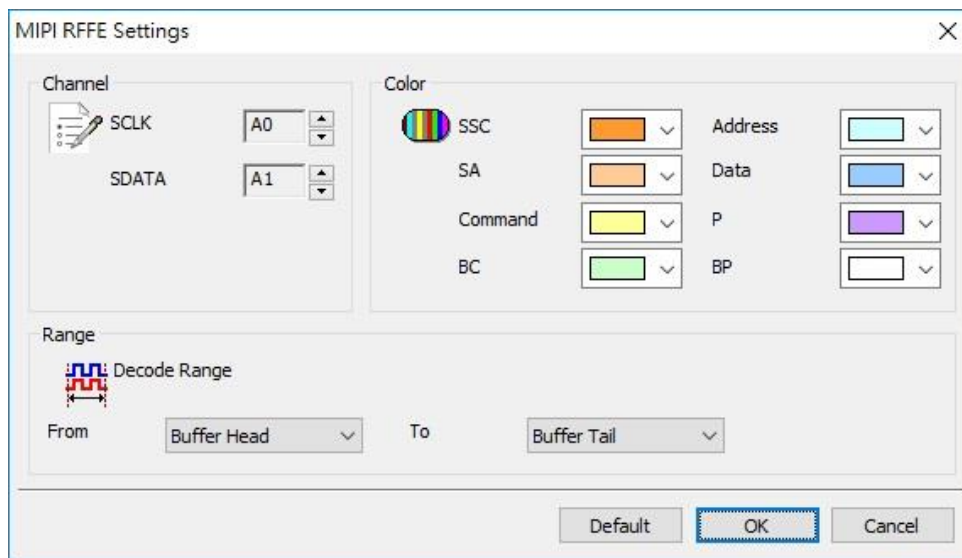
Advanced Decode Enabled:



MIPI RFFE

MIPI RFFE (RF Front-End Control Interface) designed by MIPI alliance is for controlling RF front-end devices including Power Amplifiers, Low-Noise Amplifiers, filters, switches, power management modules, antenna tuners and sensors.

Settings



Channel: Set the channels of SCLK and SDATA.

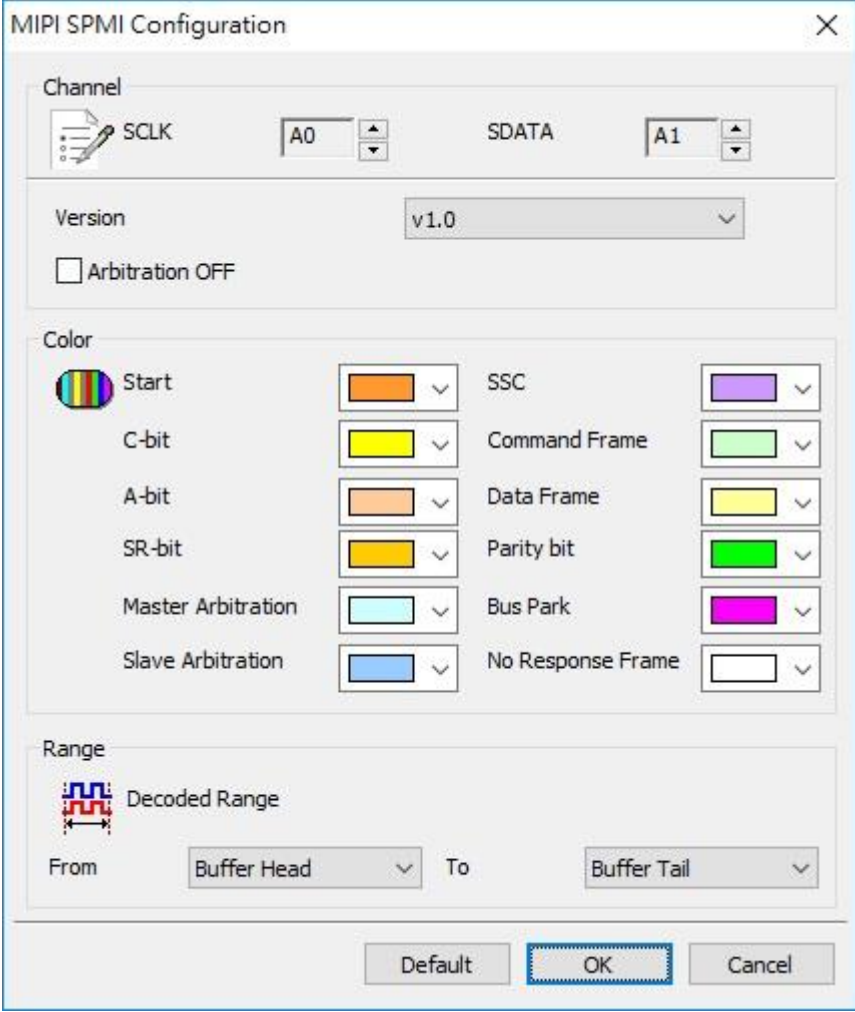
Result



MIPI SPMI

MIPI SPMI(System Power Management Interface) designed by MIPI alliance. SPMI is a serial interface that connects the integrated Power Controller(PC) with Power management Integrated Circuits(PMIC).

Settings



The image shows the 'MIPI SPMI Configuration' dialog box. It has a title bar with a close button. The dialog is divided into several sections: 'Channel' with SCLK (A0) and SDATA (A1) dropdowns; 'Version' with a 'v1.0' dropdown and an 'Arbitration OFF' checkbox; 'Color' with a grid of color selection buttons for Start, C-bit, A-bit, SR-bit, Master Arbitration, Slave Arbitration, SSC, Command Frame, Data Frame, Parity bit, Bus Park, and No Response Frame; and 'Range' with a 'Decoded Range' icon and 'From' (Buffer Head) and 'To' (Buffer Tail) dropdowns. At the bottom are 'Default', 'OK', and 'Cancel' buttons.

Channel	SCLK	SDATA
	A0	A1

Version: v1.0

☐ Arbitration OFF

Color	Start	C-bit	A-bit	SR-bit	Master Arbitration	Slave Arbitration	SSC	Command Frame	Data Frame	Parity bit	Bus Park	No Response Frame
	[Color]	[Color]	[Color]	[Color]	[Color]	[Color]	[Color]	[Color]	[Color]	[Color]	[Color]	[Color]

Range: Decoded Range

From: Buffer Head To: Buffer Tail

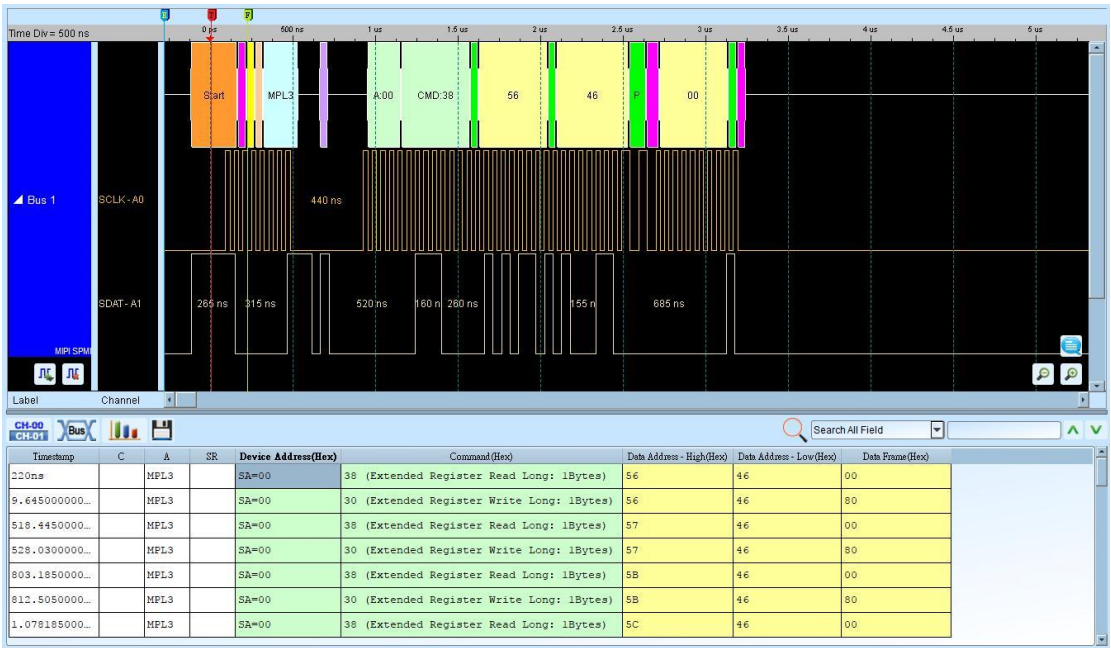
Default OK Cancel

Channel: Set the channels of SCLK and SDATA.

Result

Click OK to run the MIPI SPMI Decode and see result on the Waveform Windows

below.



MMC

The Multi Media Card (MMC) or the Embedded Multi Media Card (eMMC) version 5.0 is a flash memory card standard.

Settings

MMC Settings

Channel

Channel

CLK A0 Data3 A5

CMD A1 Data4 A6

Data0 A2 Data5 A7

Data1 A3 Data6 A8

Data2 A4 Data7 A9

DS A10

Analysis

☒ Command only

☐ Data only

☐ Command + Data

Command

☐ Ref. Data0

☐ Adv. Report

☐ Don't care clock

Data

☐ 8-bit Data

☐ 4-bit Data

☒ 1-bit Data

☐ DDR mode

☐ Non-interleaved

☐ Data Strobe

Color

Start bit

Host

Device

CMD/Resp

Argument

CRC check

End bit

Data

CRC status

Busy

Data length

512 Bytes (Min: 1, Max: 16384)

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data

Command + Data: Analyze Command and Data in the report window.

Ref. DAT0: To help analyze the R1/R1b of the response.

Adv. Report: To analyze the command argument.

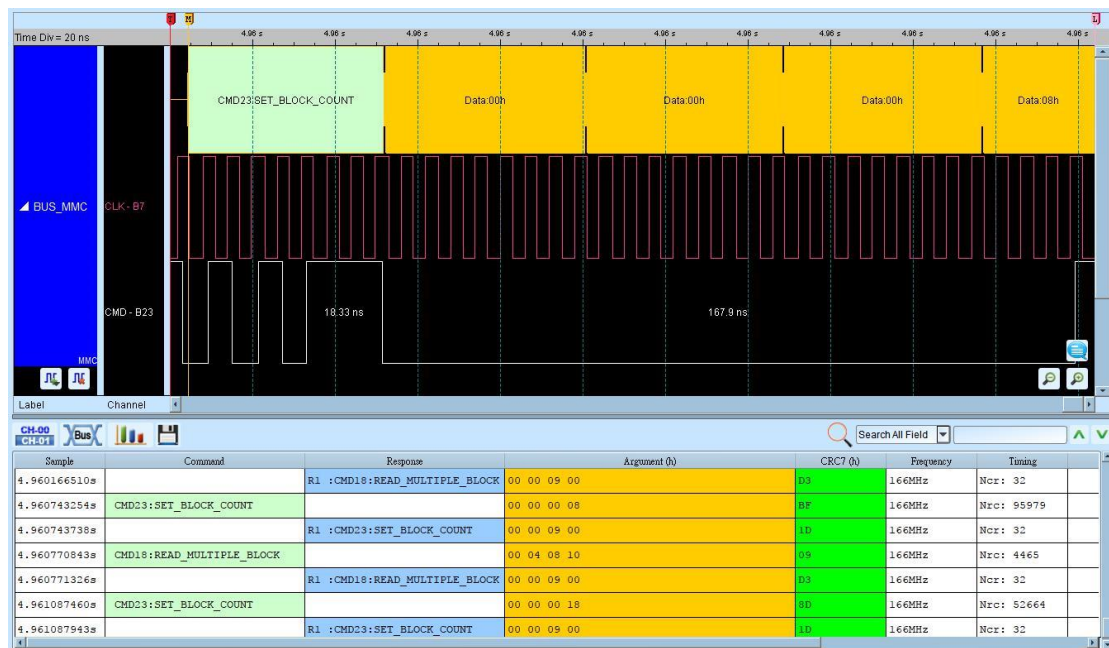
Don't care clock: To decode only depend on the CMD channel without the CLK channel.

Data: 1/4/8 bits or DDR mode, check “DDR mode” and ” “Non-interleaved” to analyze data without interleaved. Check “Data Strobe” to analyze data with the DQS channel.

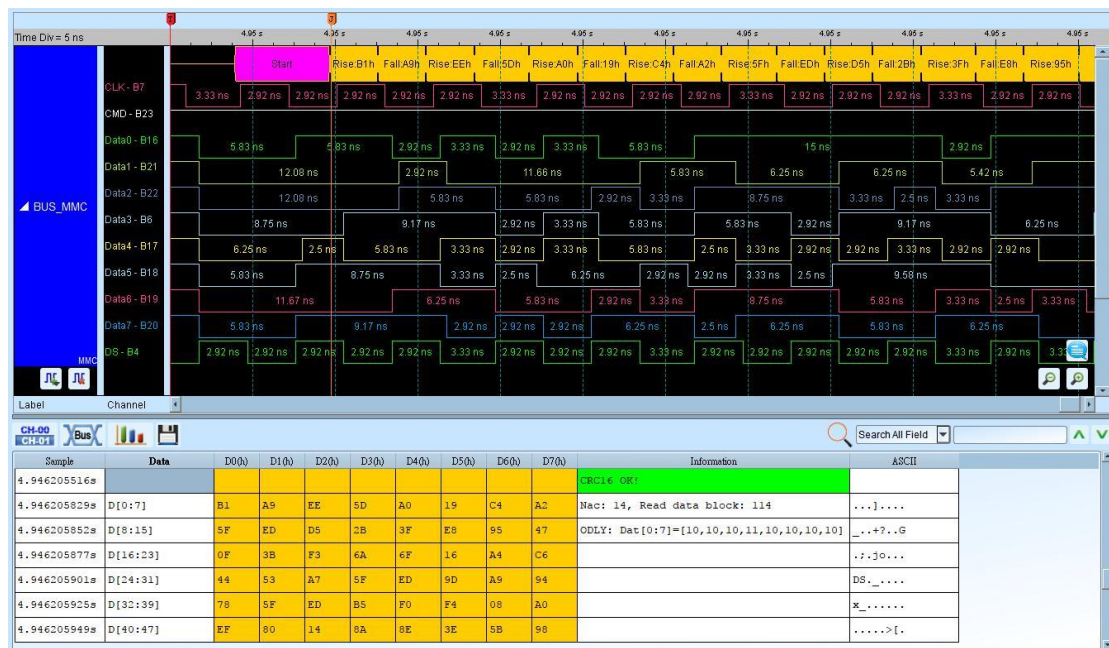
Data length: Set the number of data bits.

Result

Command:



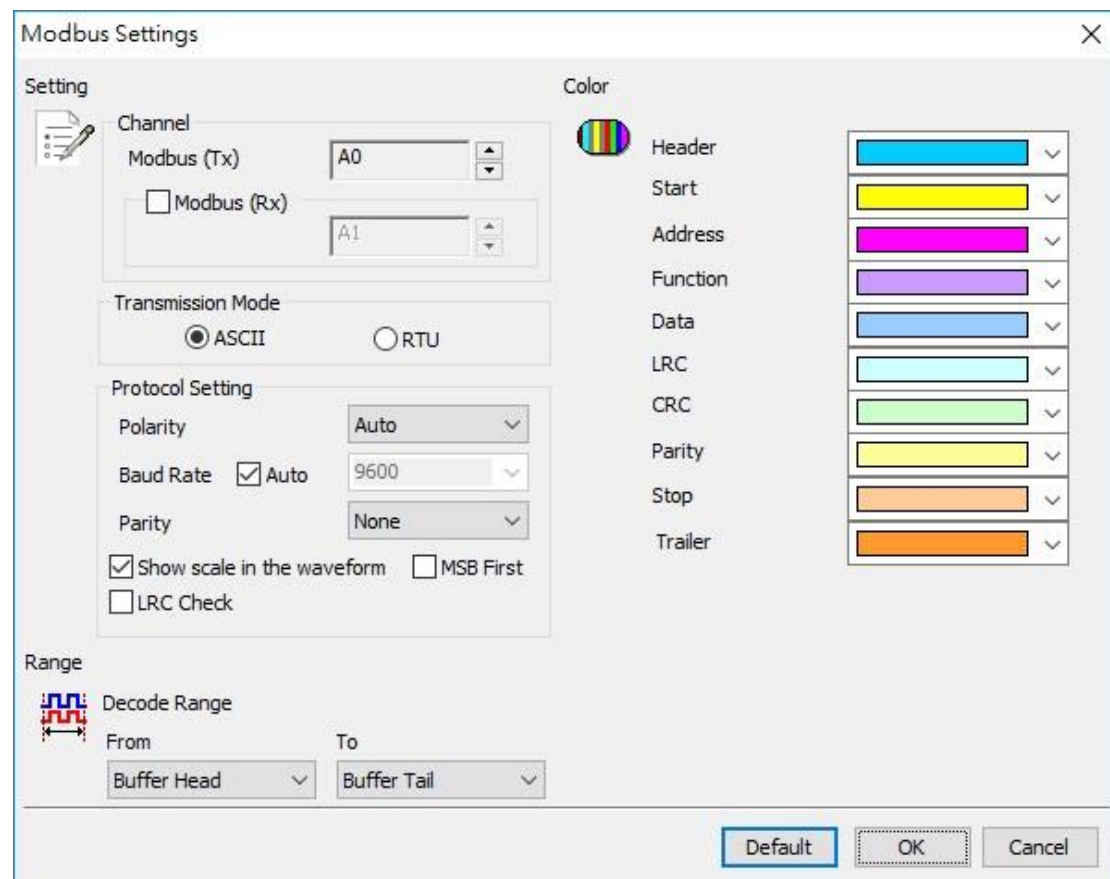
Adv. Report:



ModBus

Modbus is a serial communications protocol published by Modicon in 1979 for use with its programmable logic controllers (PLCs). Simple and robust, it has since become one of the standard communications protocols in the industry, and it is now amongst the most commonly available means of connecting industrial electronic devices.

Settings



The image shows a 'Modbus Settings' dialog box with a close button (X) in the top right corner. The dialog is divided into several sections:

- Setting**: Contains a 'Channel' section with 'Modbus (Tx)' set to 'A0' and an unchecked 'Modbus (Rx)' set to 'A1'. Below this is the 'Transmission Mode' with 'ASCII' selected (radio button) and 'RTU' unselected. The 'Protocol Setting' section includes 'Polarity' set to 'Auto', 'Baud Rate' with 'Auto' checked and '9600' selected, 'Parity' set to 'None', and checkboxes for 'Show scale in the waveform' (checked), 'MSB First' (unchecked), and 'LRC Check' (unchecked).
- Color**: A section with a color wheel icon and a list of color-coded fields: Header (blue), Start (yellow), Address (magenta), Function (purple), Data (light blue), LRC (cyan), CRC (light green), Parity (yellow), Stop (orange), and Trailer (dark orange). Each field has a corresponding color bar and a dropdown arrow.
- Range**: Contains a 'Decode Range' section with a waveform icon. It has 'From' and 'To' dropdowns, both currently set to 'Buffer Head' and 'Buffer Tail' respectively.

At the bottom right, there are three buttons: 'Default' (highlighted with a blue border), 'OK' (dashed border), and 'Cancel'.

Channel: Modbus (Tx) or Modbus (Rx).

Transmission Mode: ASCII and RTU mode.

Auto: Auto detection idle polarity.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

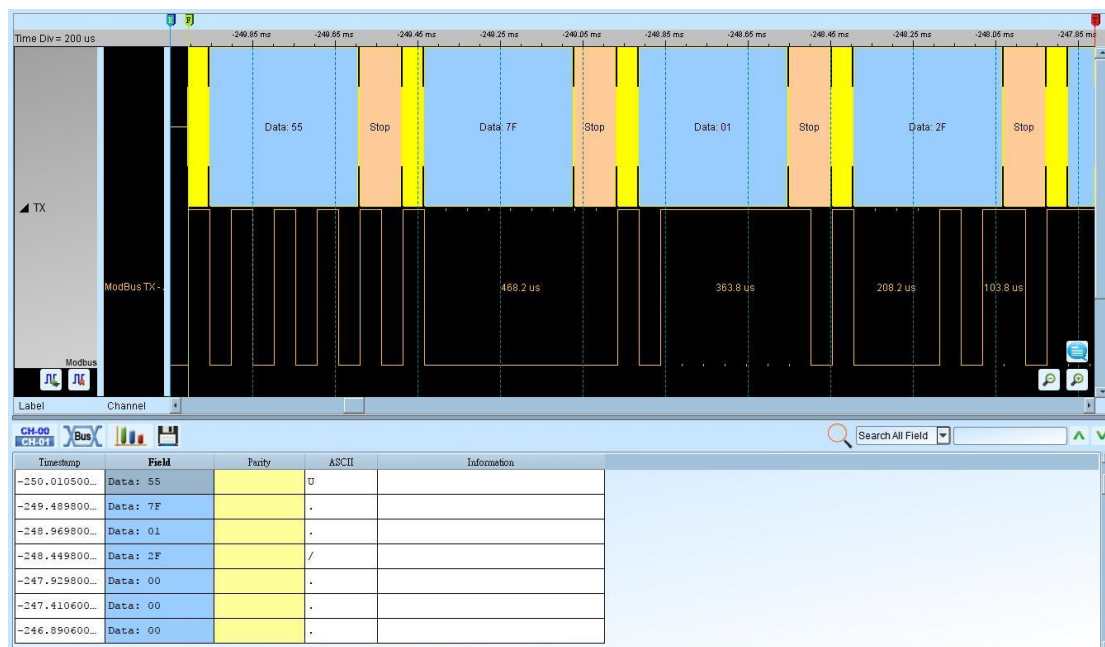
Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Parity: N-None Parity, O-Odd Parity, E-Even Parity.

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Display the waveforms with scales.

Result



NAND Flash

NAND flash uses tunnel injection for writing and tunnel release for erasing. NAND flash memory forms the core of the removable USB storage devices known as USB flash drives, as well as most memory card formats and solid-state drives available today.

Settings

NAND Flash Settings

Setting

Channel

Device Width: ☒ x8 ☐ x16

☒ I/O Quick Setup ☐ I/O User Defined

I/O (LSB): A0

I/O [A7:A0]: A0

CLE: A8

ALE: A9

RE#: A10

WE#: A11

DQS: A30

Command Latch Cycle

tDS >= 5.0ns

tDH >= 5.0ns

Data Out Cycles

tREA >= 20.0ns

tDQSQ >= 0.5ns

The Flash Startup mode

☐ Toggle / ONFI DDR Mode

Device information

Vendors: Macronix

Model: MX30LF1208AA

Color

Command: [Purple]

Address: [Orange]

Busy: [Yellow]

Data In: [Green]

Data Out: [Cyan]

Range

Decode Range

From: Buffer Head

To: Buffer Tail

Save the NAND Flash Data

Reduced Report

Show the DDR Data Output / Input Timing

Don't care R/B# signal

Reduced Command in the waveform window

Reverse RE#(W/R#)

Reverse DQS

Don't care CE# signal

Don't care ALE signal

Default OK Cancel

Channel:

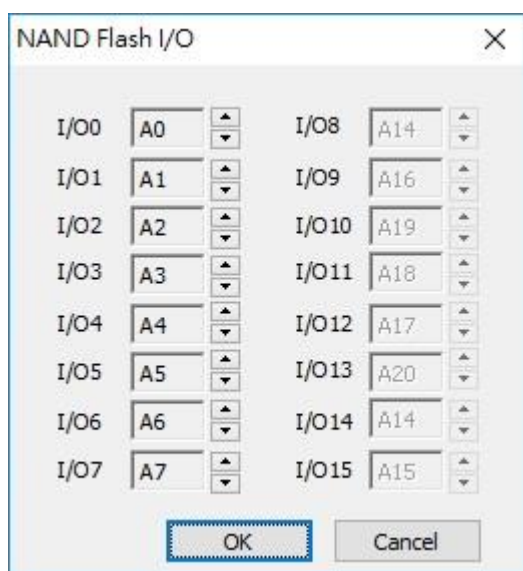
Async	Ssync	Description
I/Ox	DQx	NAND Flash data channels
CLE	CLE	Command Latch Enable channel
ALE	ALE	Address Latch Enable channel
RE	W/R	Read Enable and Write/Read channel

WE	CLK	Write Enable and Clock channel
RB#	RB#	Ready/Busy channel
CE#	CE#	Chip Enable channel
---	DQS	Data Strobe channel

Device Width: Select 8/16 bits device width.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

I/O Quick Setup / I/O User Defined: Only set I/O0 (LSB) when select the I/O Quick Setup, other channels will be set automatically. when check the I/O User Defined and press the button will show the dialog below:



User can set NAND I/O channel by channel.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

t_{REA} / t_{DQSQ}: Set the delay time to access the NAND data under SDR / DDR **Save**

the NAND Flash Data: Save the read/write data. Program will save the NAND Flash read/write data as a file when check Save the NAND Flash Data. It will be saved into the LA work directory.

mode.

Reduced Report: Only show NAND Flash command in the Report window when check it.

Show the DDR Data Output/Input Timing: Only show timing information under DDR mode.

Reduced Command in the waveform window: Only show NAND Command value in the waveform window.

Don't care ALE/RB#/CE# signal: Ignore the signal selected when decode.

Description of file name as following:

File Name	Description
NF_DI/NF_DO	NAND Flash Data In / Data Out
_Rowxxxxxxh	Row Address
_Colxxxxh	Column Address
CEx	Active CEx
_1, _2, _3	File Order

Ex:NF_DI_Row017821h_Col0000h_CE1_1.bin

NF_DO_Row017821h_Col0000h_CE1_2.bin

NF_DO_Row_Col_CE1_3.bin

Compare the content of file with the one of report.

D0	D1	D2	D3	D4	D5	D6	D7
5A	A6	6F	36	B2	38	B8	B7
06	8A	B7	0B	B1	19	C8	21
7E	CE	58	EF	BD	18	47	7C
5E	DD	9A	E3	A5	E4	02	11
E9	2D	96	14	86	32	CE	F4
53	10	60	79	EA	B6	D6	CE
5A	22	53	A5	F1	9E	DB	58
8A	73	B3	B1	82	19	B9	46
92	25	76	EA	E4	CE	74	A7
1C	E5	20	3D	9F	74	BB	E5
55	54	68	4C	69	86	AC	0F

```

000000 5A A6 6F 36 B2 38 B8 B7 06 8A B7 0B B1 19 C8 21
000010 7E CE 58 EF BD 18 47 7C 5E DD 9A E3 A5 E4 02 11
000020 E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE
000030 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46
000040 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
000050 55 54 68 4C 69 86 AC 0F F1 A2 47 FA 37 4B 04 0D

```

Device information

Vendors: Select the NAND Flash Vendor. Please refer to the following details when select the **Custom** item.

Model: Select the NAND Flash device type.

Custom: Users create a **AqNFCustom.txt** file into the LA work directory when select the **Custom** vendor item and edit NAND Flash Command set.

```

Manufacturer=Samsung
PartNo=K9XXXXXXXX
#CE/RB=1
X16=N
SyncMode=Y
Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30
Cmd=Read Status, Read Stat., , , , Y, N, Y, 70
Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000, N, Y, N, 80, 11, 81, 10

```

Manufacturer, PartNo, #CE/RB, X16, SyncMode, Cmd are keywords.

Keyword	Description
Manufacturer	NAND Flash Vendor.
PartNo	NAND Flash IC Model.
#CE/RB	Number of targets, only 1/2/4 acceptable.
X16	8/16 bits device width, only Y/N acceptable.
SyncMode	Only Y/N acceptable, Y: Synchronous data interface supported; N: Not supported.
	Cmd is composed of several parts, it's divided with comma.
	1. Complete command name.
	2. Abbreviation of command.
	Name of first busy time check. Put a space and add a comma if unused.
	Value of first busy time check. Its unit is micro seconds. Put a space

	and add a comma if unused.
	Name of second busy time check. Put a space and add a comma if unused.
	Value of second busy time check. Its unit is micro mseconds. Put a space and add a comma if unused.
	First flag. It's acceptable command during busy.
	Second flag. It can be inserted by some command or not.
	Third flag. It can insert into some multi plane command or not.
	Command.

Ex: Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30

Cmd=Read Status, Read Stat., , , , Y, N, Y ,70

Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000,
N, Y, N, 80, 11, 81, 10

Read Status / Two-Plane Page Program : complete command.

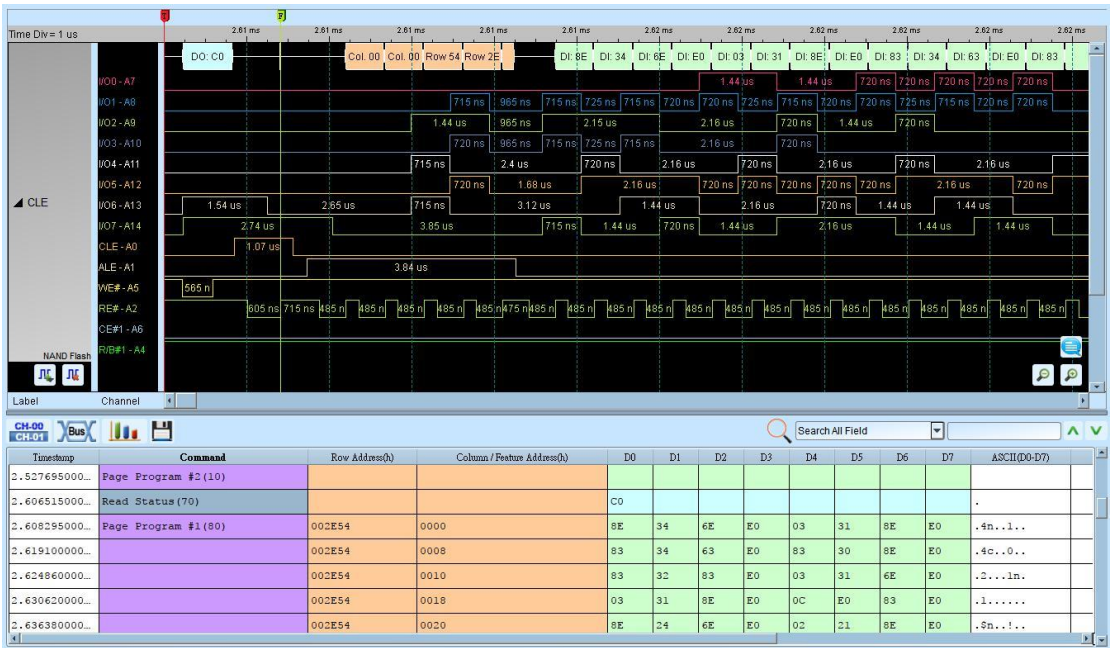
Read Stat. / TPP Prog. : abbreviation of command.

Busy Time Check(tDBSY, 1, tPROG, 5000) : tDBSY is 1us; tPROG is 5000 us. It will show some information when violation of busy time.

3 Flags: 1st flag of "Read Status" is Y means it's acceptable command

During busy; 2nd flag of "Two-Plane Page Program" and 3rd flag of "Read Status" means any command between 11h and 81h is prohibited except "Read Status (70h)".

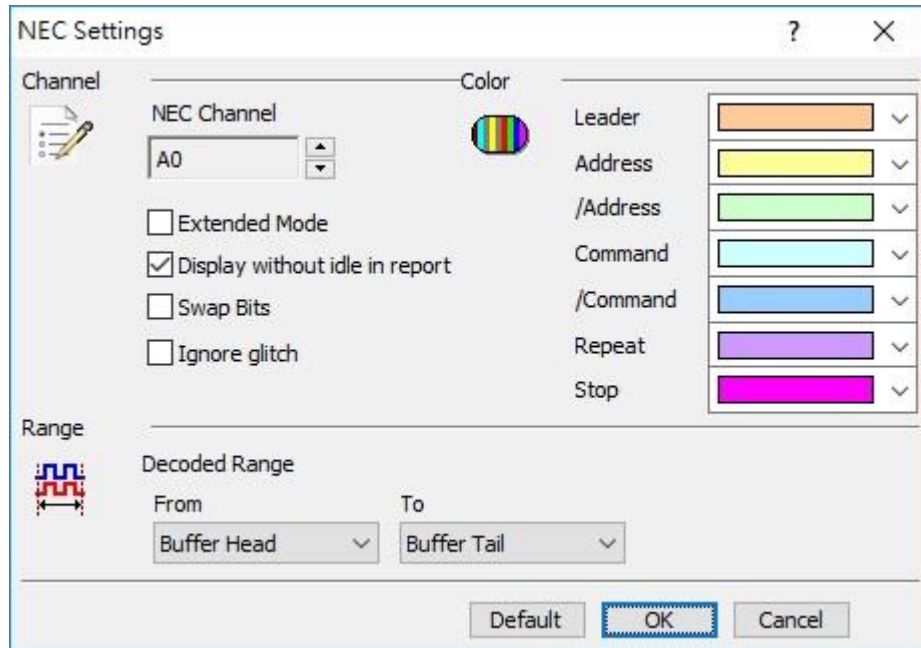
Result



NEC IR

It needs only one channel to analysis NEC signals.

Settings



Channel: Display the channel (CH 0).

Extended Mode: It integrates /Address and Address into 16 Bits Address, /Command and Command into 16 Bits Command.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Swap Bits: Switch LSB First to MSB First.

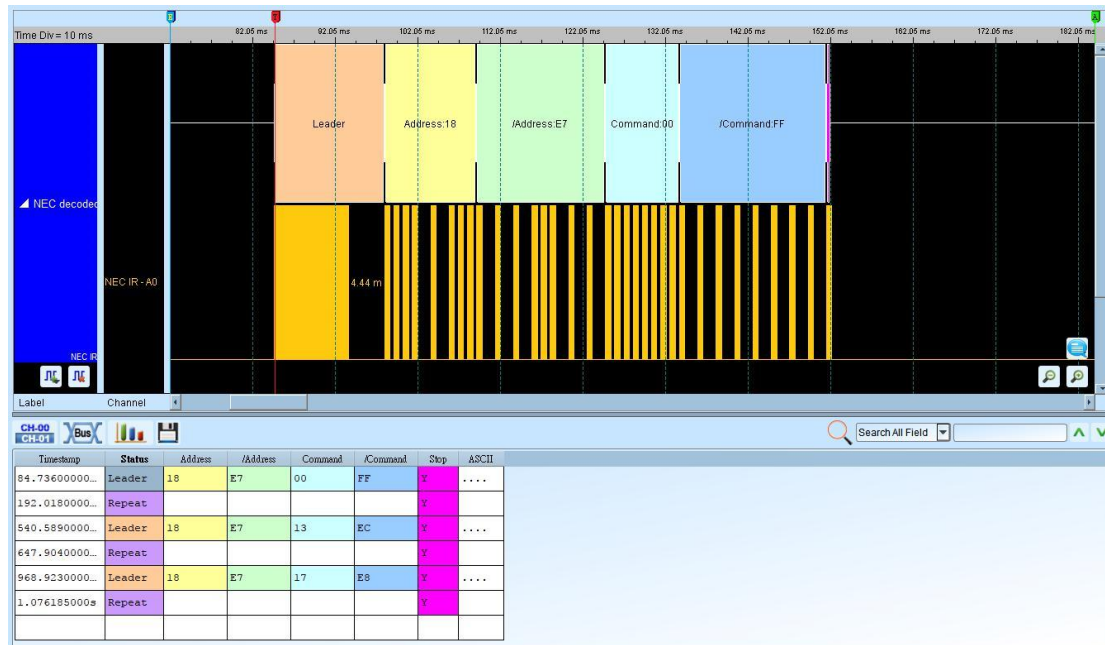
Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Result

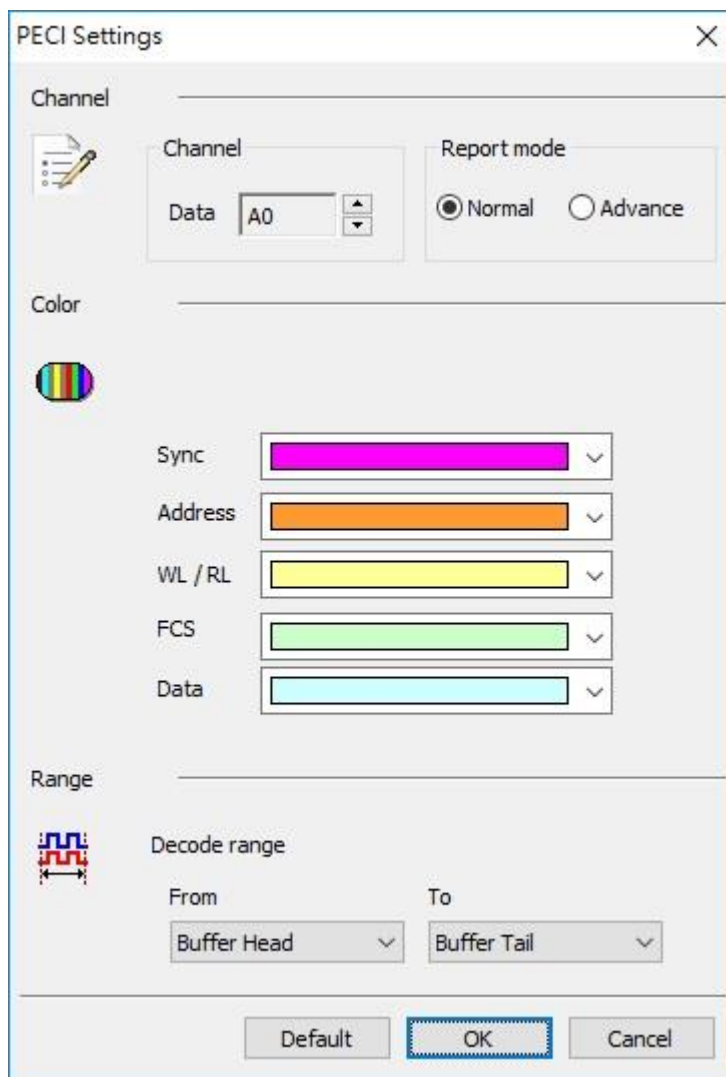
Click **OK** to run the NEC IR decode and see the result on the Waveform Window below.



PECI

Platform Environment Control Interface, Platform management include thermal, power and electrical error monitoring.

Settings



The image shows a 'PECI Settings' dialog box with a close button (X) in the top right corner. The dialog is organized into three main sections: Channel, Color, and Range.

- Channel Section:** Contains a 'Channel' label, a 'Data' dropdown menu currently set to 'A0', and a 'Report mode' section with two radio buttons: 'Normal' (selected) and 'Advance'.
- Color Section:** Features a color selection icon (a circle with vertical rainbow bars) and five color-coded dropdown menus: 'Sync' (magenta), 'Address' (orange), 'WL / RL' (yellow), 'FCS' (light green), and 'Data' (light blue).
- Range Section:** Includes a 'Range' label, a waveform icon, and a 'Decode range' section with 'From' and 'To' dropdown menus, both currently set to 'Buffer Head' and 'Buffer Tail' respectively.

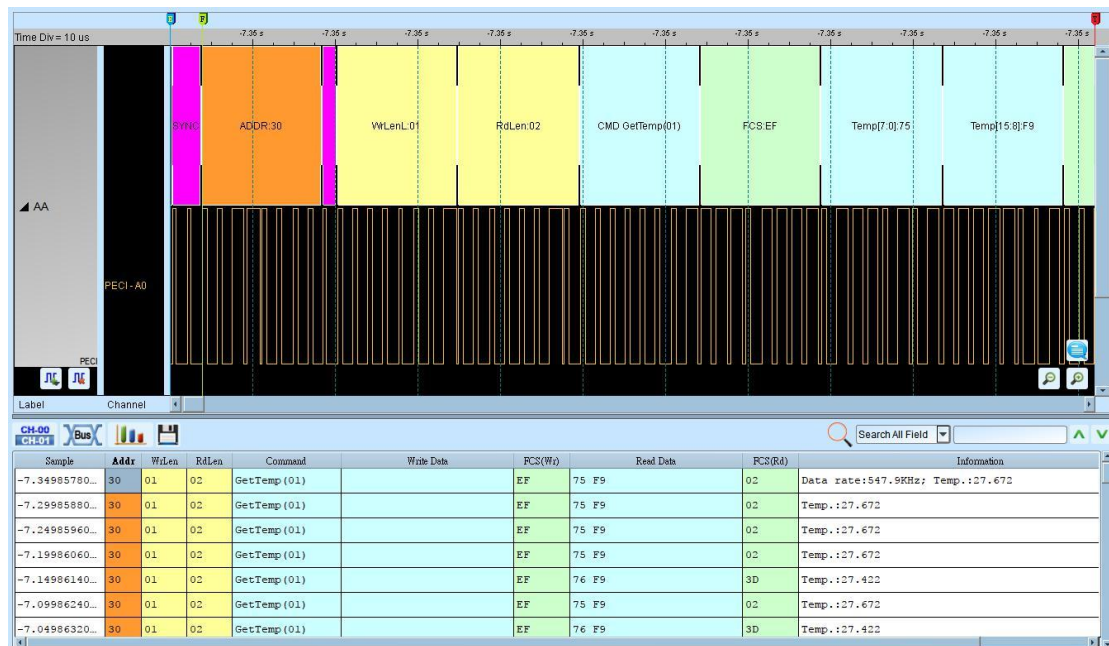
At the bottom of the dialog are three buttons: 'Default', 'OK' (which is highlighted with a blue dashed border), and 'Cancel'.

Channel: Show the selected channels.

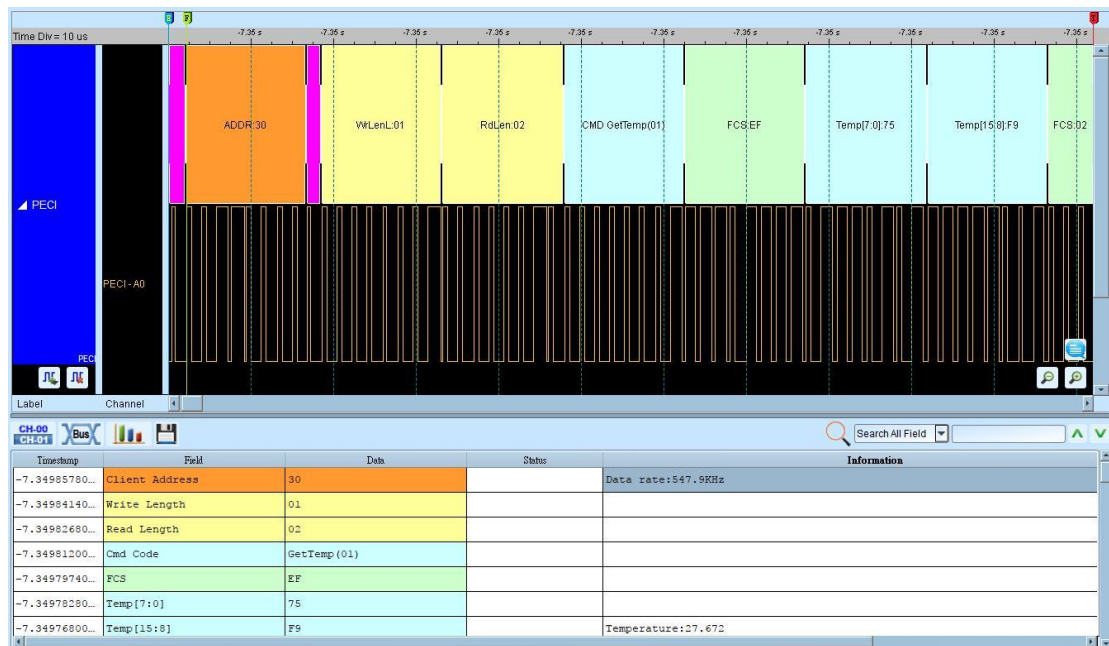
Report mode: Normal or Advance

Result

Normal mode



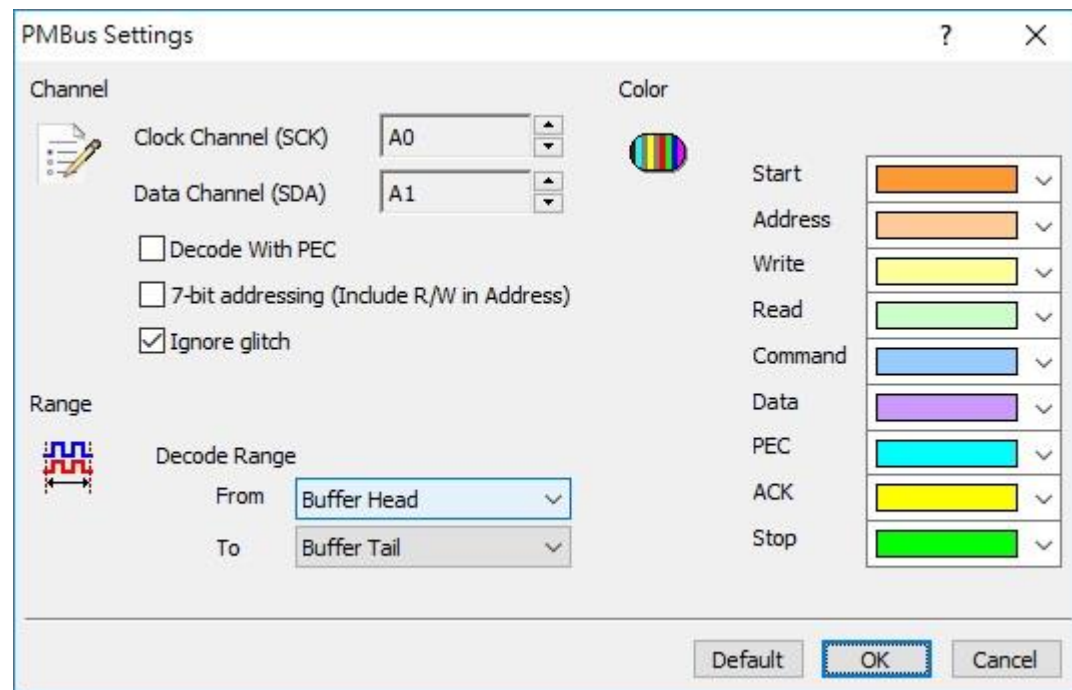
Advance mode



PMBus

The Power Management Bus (“PMBus”) is an open standard protocol that defines a means of communicating with power conversion and other devices.

Settings



Channel: Show the selected channels.

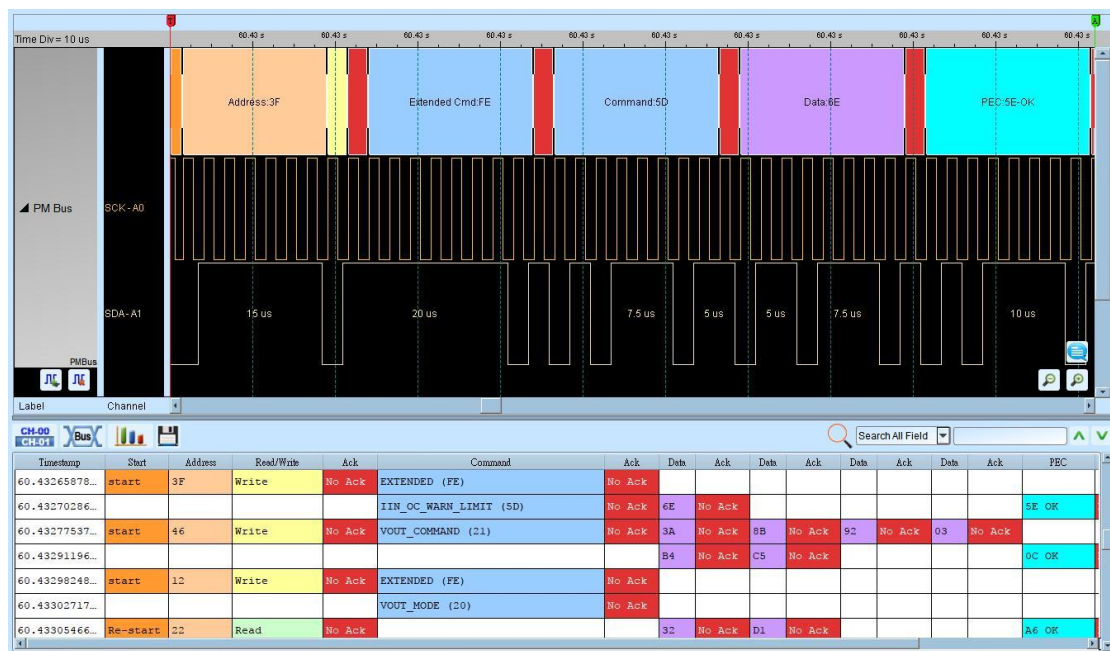
Decode With PEC: Group command protocol with PEC.

7-bit addressing (Include R/W in address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

Ignore glitch: Ignore the glitch when the slow transitions.

Result

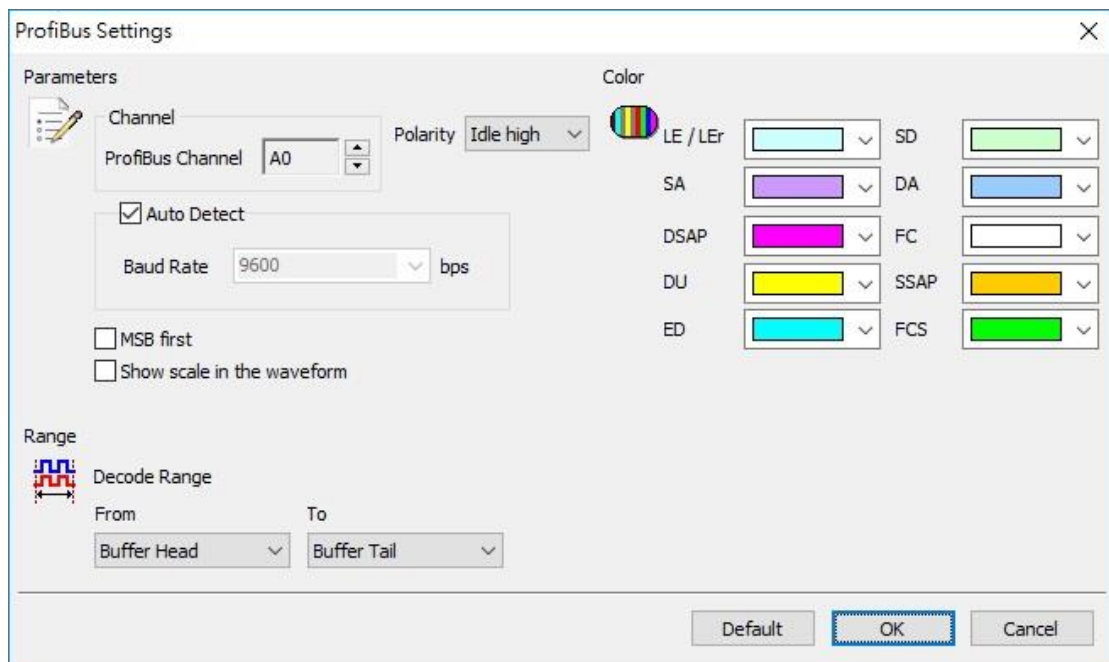
Click **OK** to run the PMBus decode and see the result on the Waveform Window below.



ProfiBus

ProfiBus (PROcess Field Bus) is implemented by RS485. It includes PROFIBUS DP, PROFIBUS PA and PROFIBUS FMS.

Settings



The image shows a 'ProfiBus Settings' dialog box with the following sections:

- Parameters:**
 - Channel:** A dropdown menu showing 'A0'.
 - Polarity:** A dropdown menu showing 'Idle high'.
 - Auto Detect:** A checked checkbox.
 - Baud Rate:** A dropdown menu showing '9600' with 'bps' next to it.
 - MSB first:** An unchecked checkbox.
 - Show scale in the waveform:** An unchecked checkbox.
- Color:** A section with a color wheel icon and a table of color-coded fields:

Field	Color
LE / LEr	Cyan
SA	Purple
DSAP	Magenta
DU	Yellow
ED	Light Blue
SD	Light Green
DA	Blue
FC	White
SSAP	Orange
FCS	Green
- Range:**
 - Decode Range:** A section with a waveform icon and two dropdown menus: 'From' (showing 'Buffer Head') and 'To' (showing 'Buffer Tail').

At the bottom right are three buttons: 'Default', 'OK' (highlighted with a blue border), and 'Cancel'.

Channel: Set the ProfiBus Channel

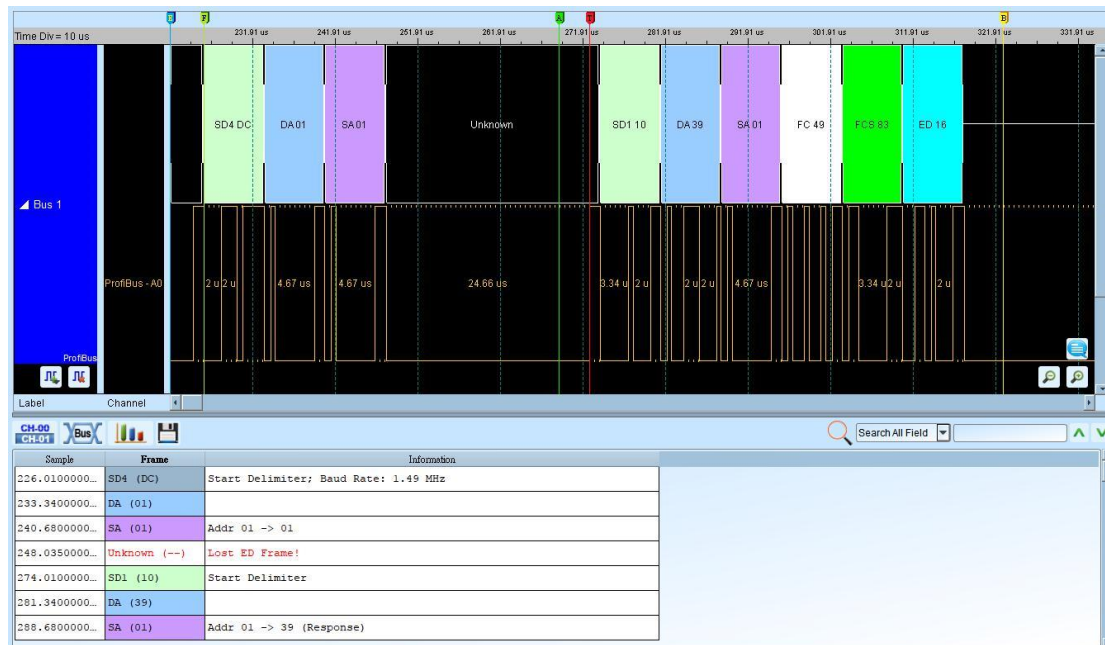
Polarity: Set the polarity Idle high / Idle low

Baud Rate/Auto Detect: Set the baud rate manually or auto detect

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Show the scale in the waveform section

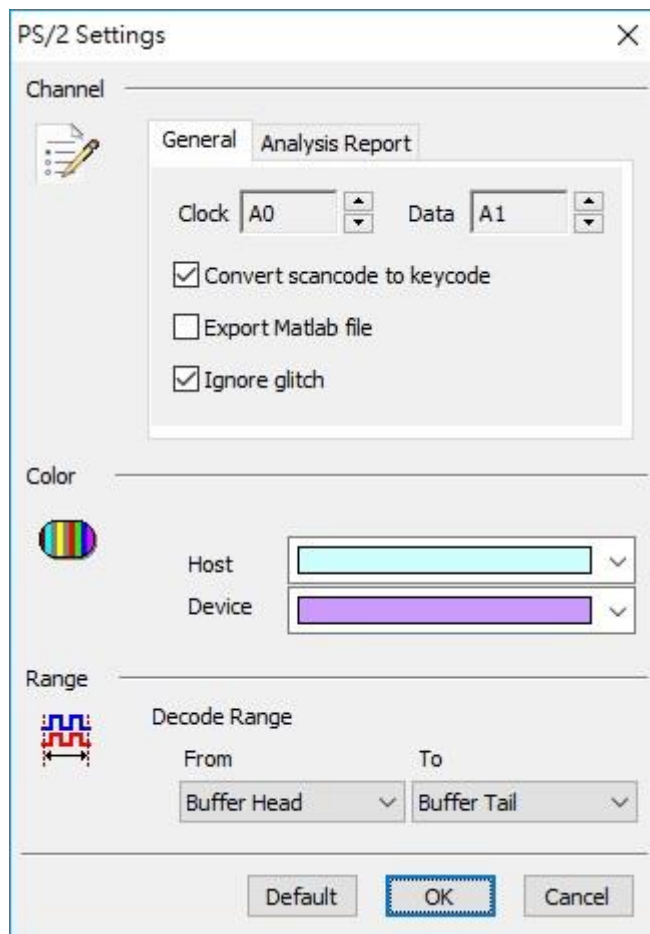
Result



PS/2

The Personal System/2 (PS/2) protocol has 6 data bits, but only the first bit (Data) and the fifth bit (Clock) need to be analyzed.

PS/2 Settings



Channel: Show the selected channels.

Convert scan code to key code: Transform data into keyboard characters.

Export MATLAB file: Export the data with MATLAB format as the following:

Time = [25.78484 25.785985 ...]

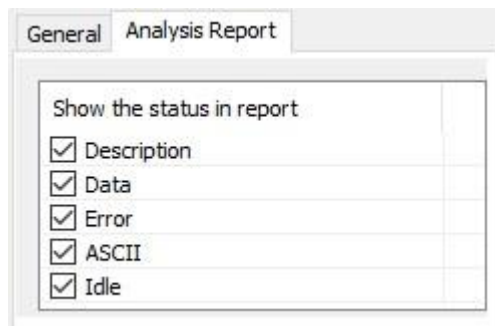
Description = [DH DH ...] DH = Device to Host, HD = Host to Device

Data = [58 FA 02 FA C4 ...]

The file (PS2_Matlab.m) will be saved at work directory

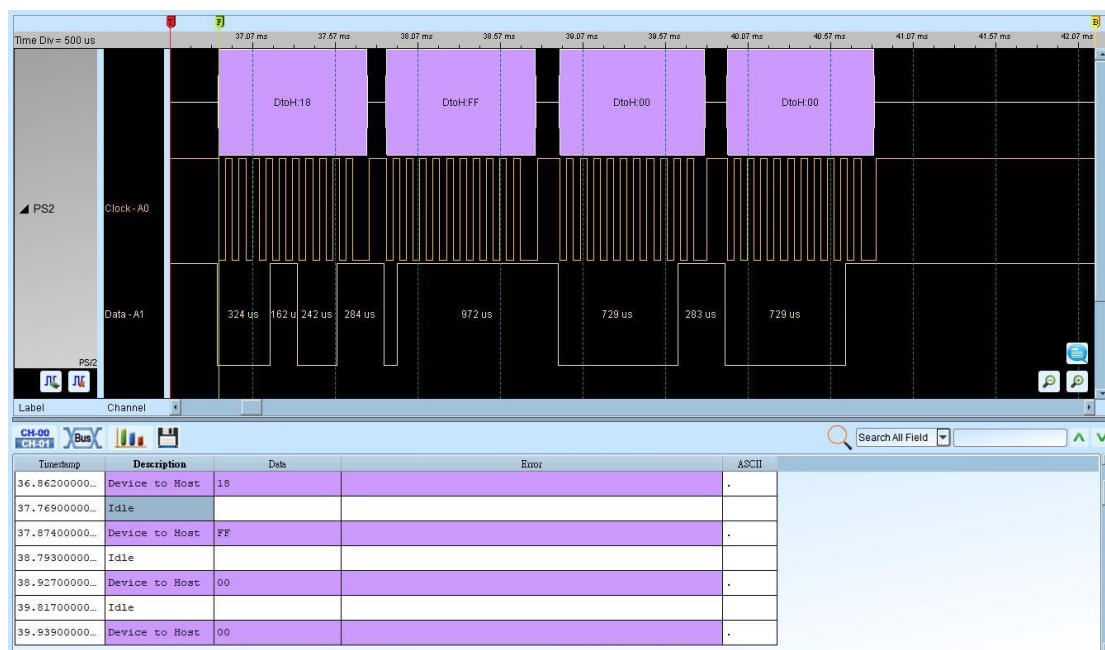
Ignore glitch: Ignore the glitch when the slow transitions.

Analysis Report: Show the selected status in report.



Result

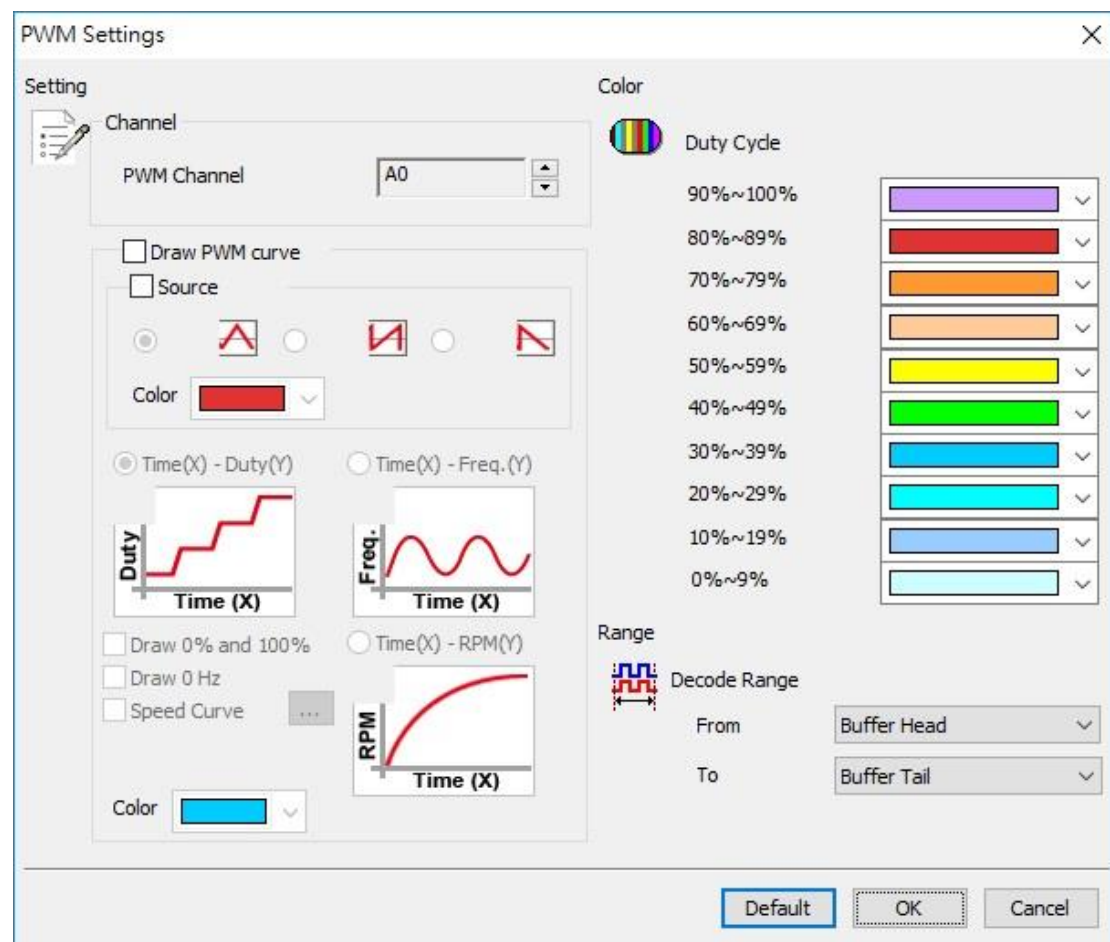
Click **OK** to run the PS/2 decode and see the result on the Waveform Window below.



PWM

Pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

Settings



Channel: Show the selected channel.

Draw PWM curve:

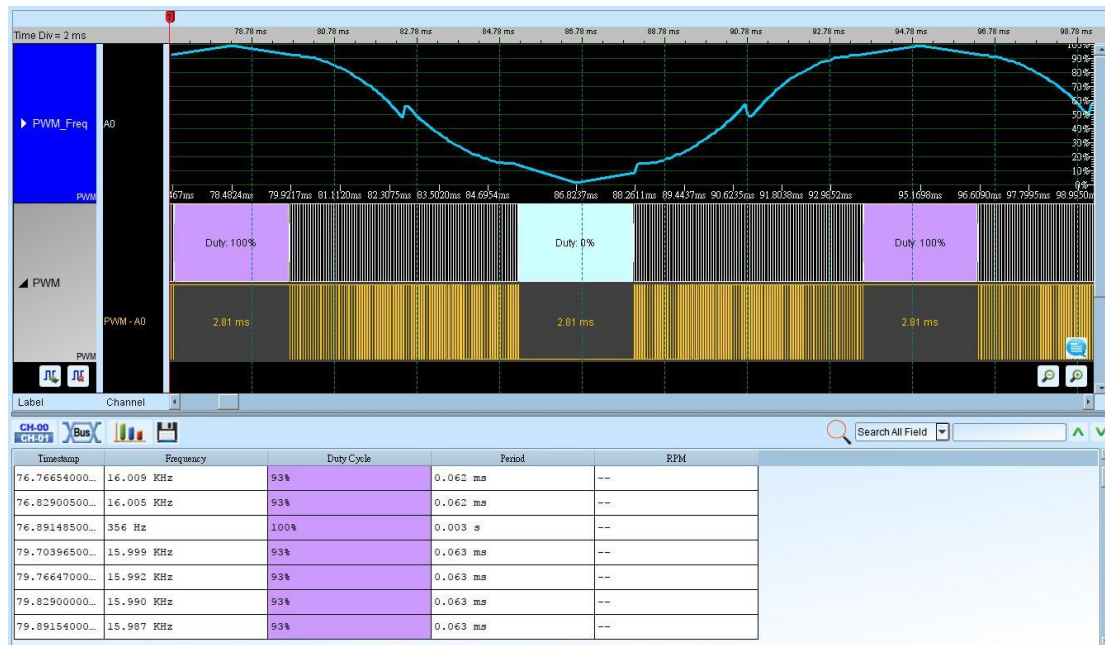
Source: Show the source waveform of the PWM.

Time(X)-Duty(Y): Show the curve diagram with Time(X) and Duty(Y)

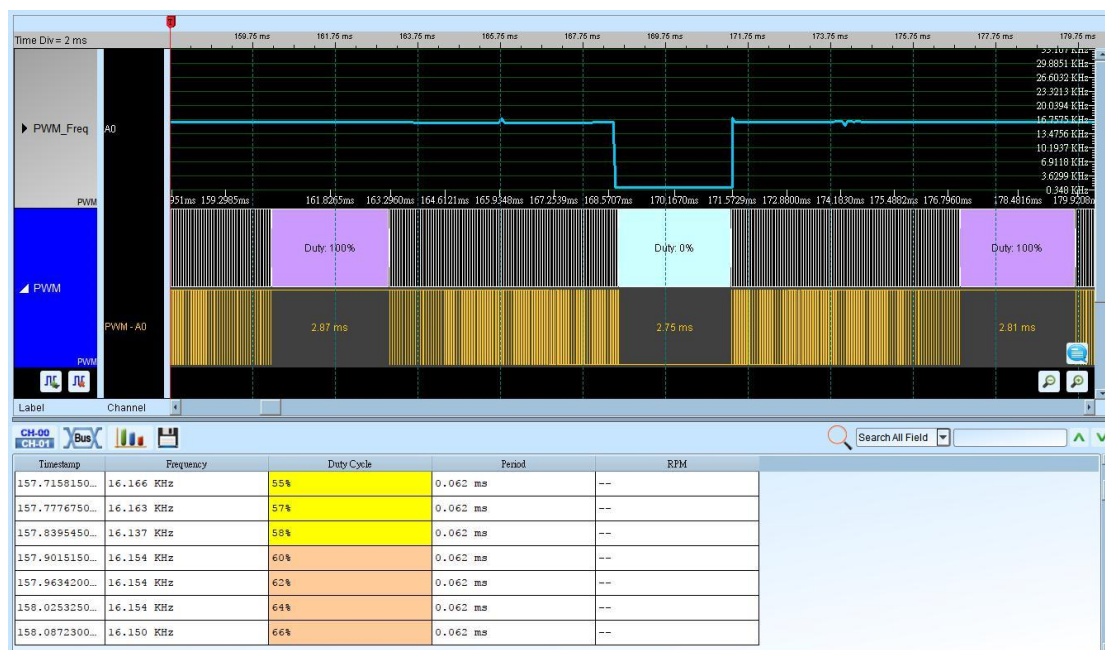
Time(X)-Freq.(Y): Show the curve diagram with Time(X) and Freq.(Y)

Time(X)-RPM(Y): Show the curve diagram with Time(X) and RPM(Y)

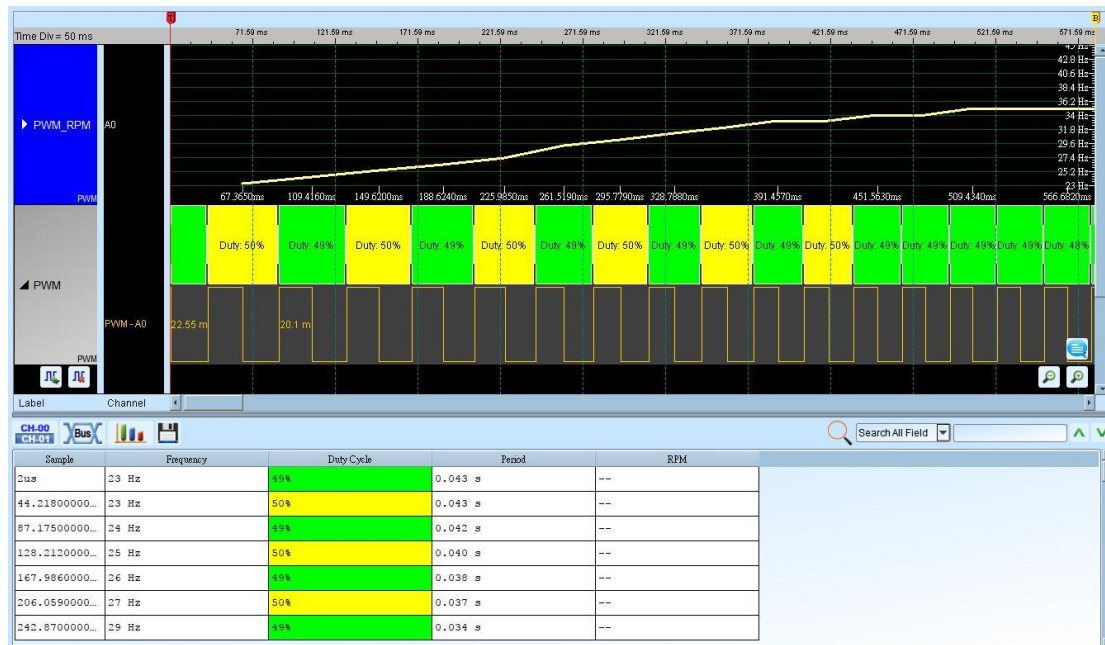
Select Time(X)-Duty(Y)



Select Time(X)-Freq.(Y)



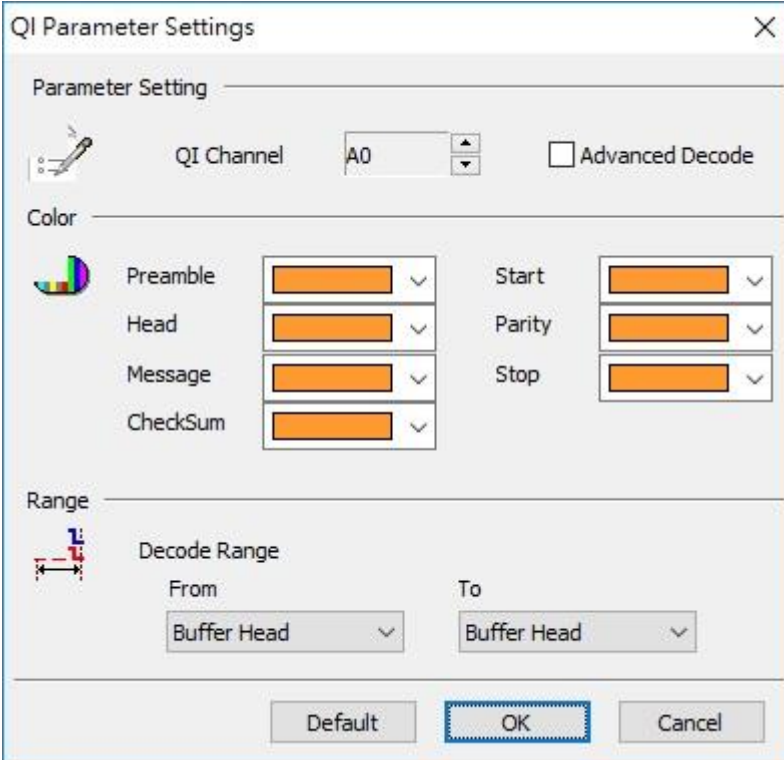
Select Time(X)-RPM(Y)



QI

QI is a contactless power transfer protocol published by Wireless Power Consortium (WPC). It is a method of contactless power transfer from a Base Station to a Mobile Device, which is based on near field magnetic induction between coils.

Settings



The image shows a 'QI Parameter Settings' dialog box. It has a title bar with a close button. The main area is divided into three sections: 'Parameter Setting', 'Color', and 'Range'. The 'Parameter Setting' section includes a 'QI Channel' dropdown menu set to 'A0' and an 'Advanced Decode' checkbox. The 'Color' section has a 'Color' icon and two columns of dropdown menus for 'Preamble', 'Head', 'Message', 'Checksum', 'Start', 'Parity', and 'Stop'. The 'Range' section has a 'Range' icon and a 'Decode Range' section with 'From' and 'To' dropdown menus, both set to 'Buffer Head'. At the bottom are 'Default', 'OK', and 'Cancel' buttons.

QI Parameter Settings

Parameter Setting

QI Channel: A0 ☐ Advanced Decode

Color

Preamble: [Dropdown] Start: [Dropdown]
Head: [Dropdown] Parity: [Dropdown]
Message: [Dropdown] Stop: [Dropdown]
Checksum: [Dropdown]

Range

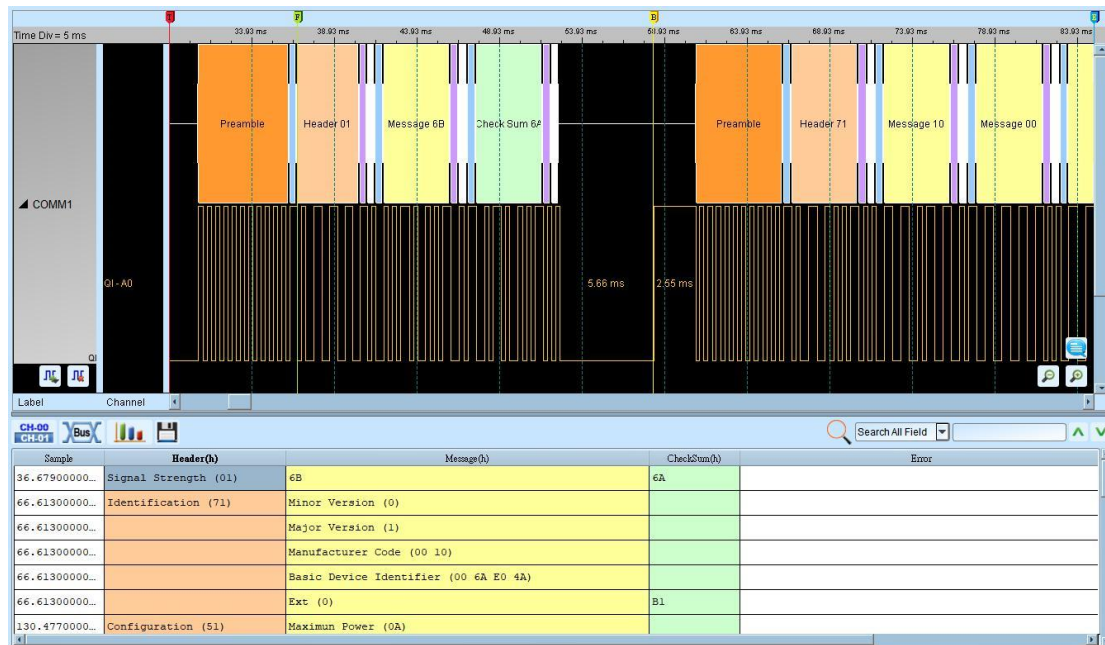
Decode Range
From: Buffer Head To: Buffer Head

Default OK Cancel

QI Channel: Show the selected channel.

Advance Decode: show detail message decode

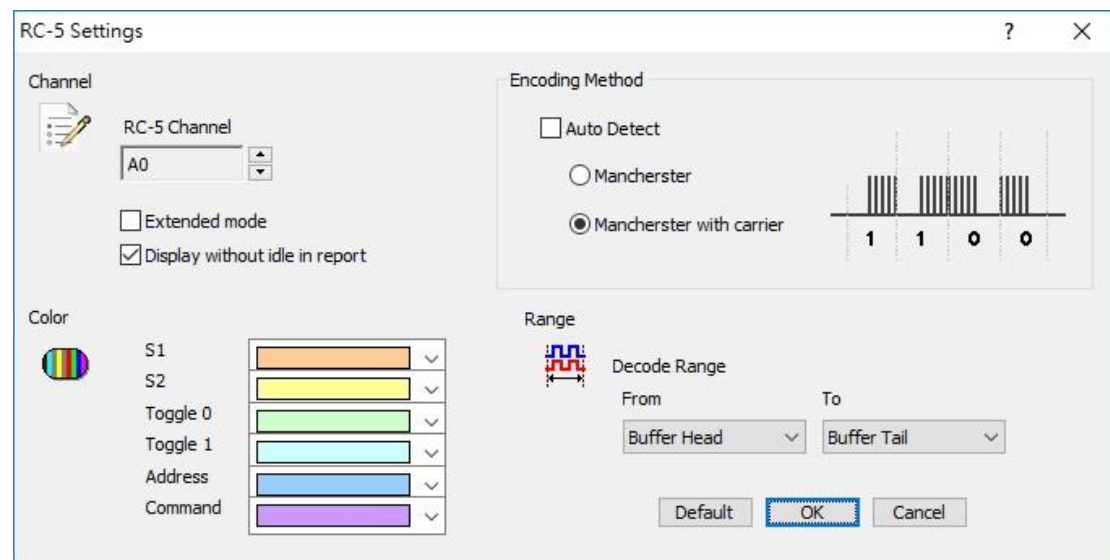
Result



RC-5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. The protocol is well defined for different device types ensuring compatibility with your whole entertainment system.

Settings



Channel: Show the selected channel (CH 0).

Extended mode: When the Extended enabled, the S2 will be converted into seventh bit of the Command. There is an Extend Command on the Waveform Window.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Encoding Method: Auto Detect mode, Manchester mode and Manchester with carrier mode.

S1/S2: Start bit.

Toggle 0/Toggle 1: The difference is that has been used while sending the message to

repeat, or send a new message.

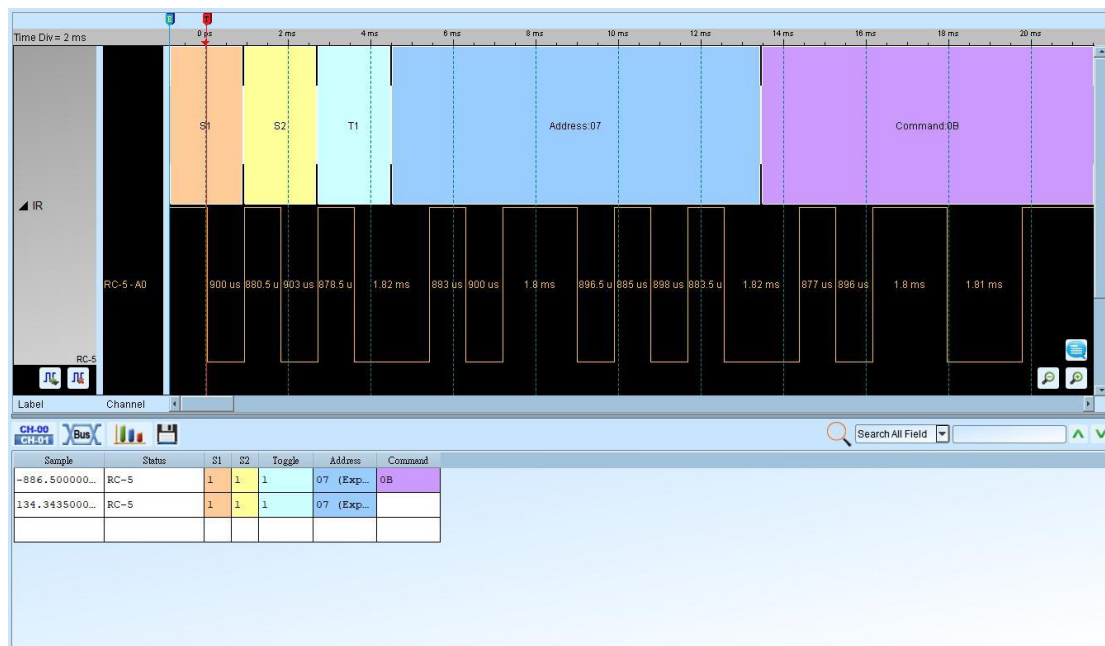
Address: To represent different device addresses.

Command: To represent the different button commands.

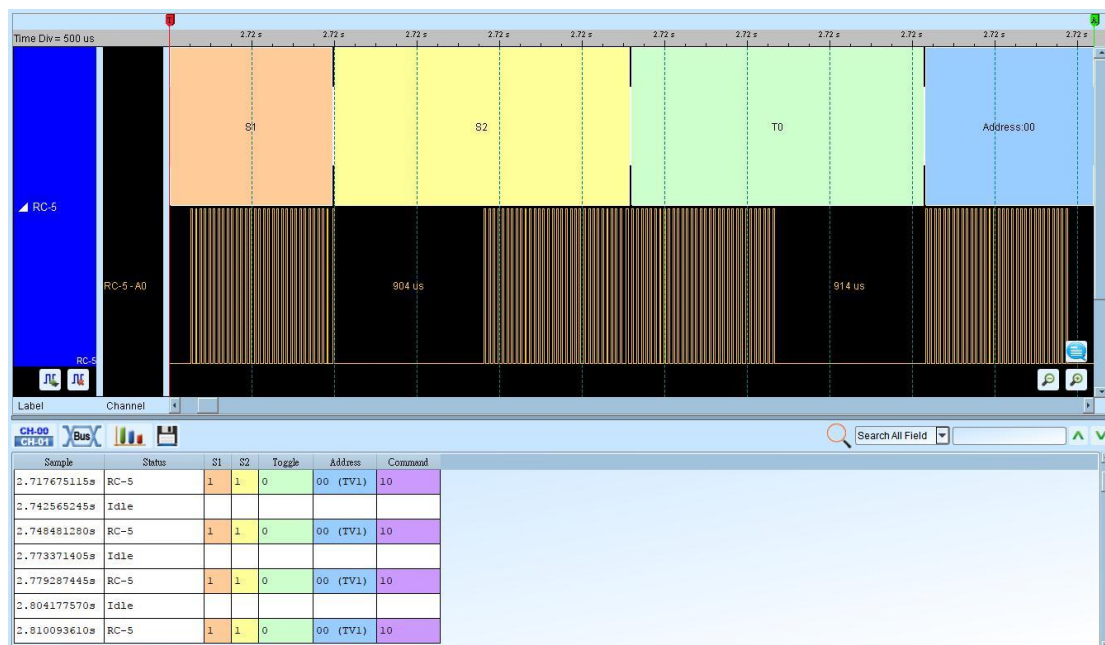
Result

Click **OK** to run the RC-5 decode and see the result on the Waveform Window below.

RC5 without carrier



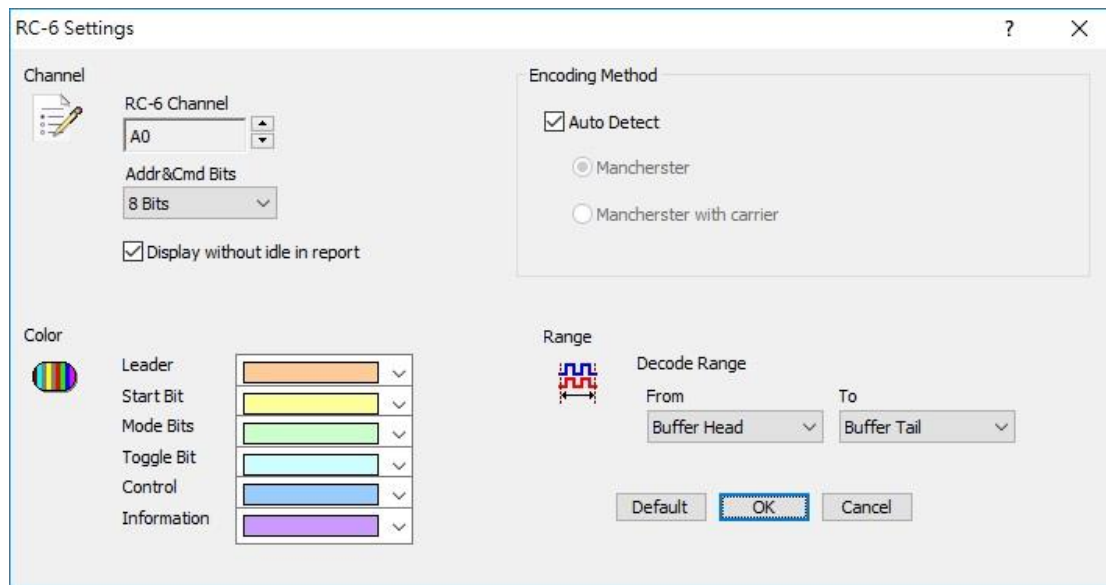
RC5 with carrier



RC-6

RC-6, like RC-5, is also developed by Philips. But, RC-6 has more features of remote controls than RC-5.

Settings



Channel: Show the selected channel (CH 0).

Add & Cmd Bits: Show commands in 8 bits or 16 bits of address and information in the control label.

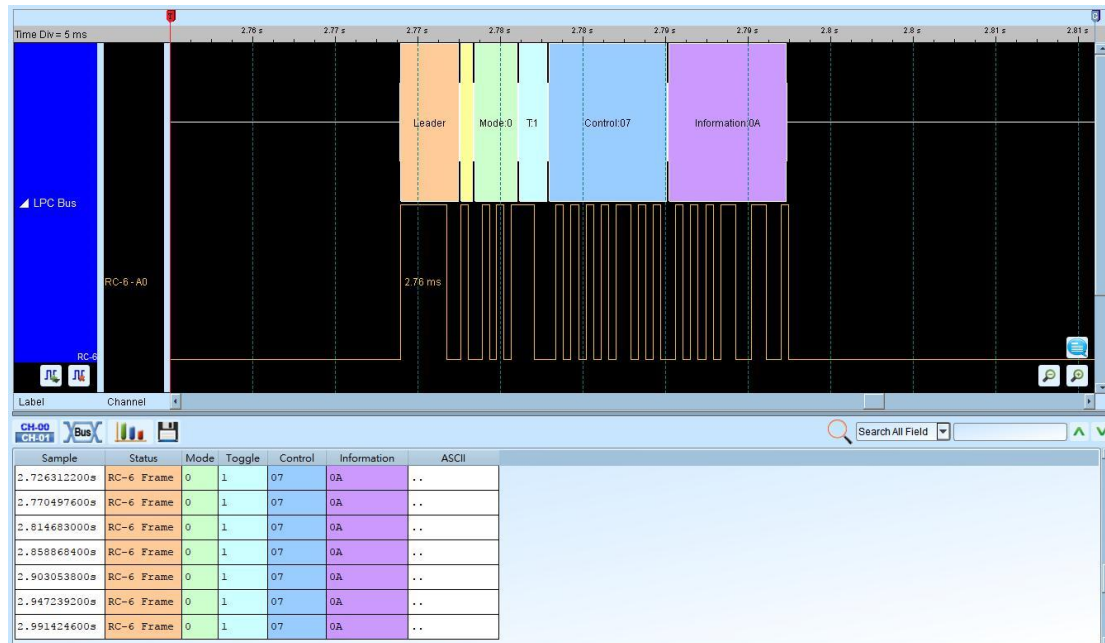
Display without idle in report: Do not display any idle in the Report Window.

Encoding Method: Auto detect mode, Manchester mode, Manchester with carrier mode.

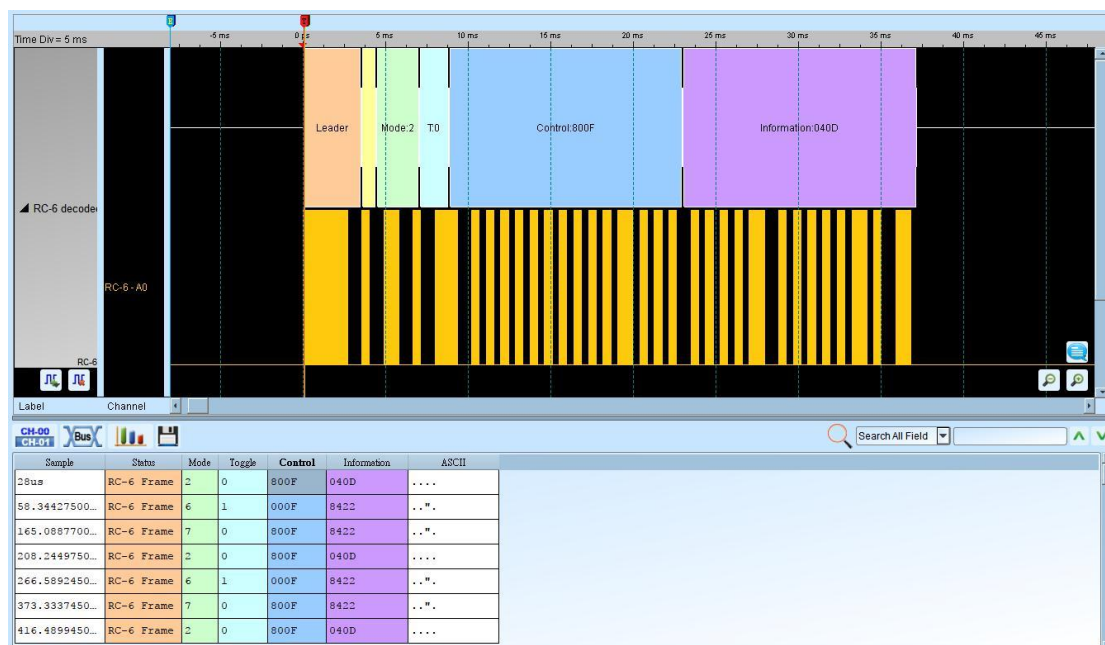
Result

Click **OK** to run the RC-6 decode and see the result on the Waveform Window below.

RC6 without carrier



RC6 with carrier



RGB Interface

RGB Interface is for data transmission between MCU and LCD. LCD Panel can be driven by LCD controller. RGB data would be written in memory and can be transmitted to LCD controller. It is able to show the picture of LCD Panel by reading the data from the interface.

Settings

RGB_IF Settings

Channel

Signal	Address Range
SCLK	A0
DE	A1
HSYNC	A2
VSYNC	A3
R0	A4
R1	A5
R2	A6
R3	A7
R4	A8
R5	A9
R6	A10
R7	A11
G0	A12
G1	A13
G2	A14
G3	A15
G4	A16
G5	A17
G6	A18
G7	A19
B0	A20
B1	A21
B2	A22
B3	A23
B4	A24
B5	A25
B6	A26
B7	A27

Format

Format: RGB888 ☐ Save as JPG file

A (Alpha) R (Red) G (Green) B (Blue) L (Luminance)

0 bits 8 bits 8 bits 8 bits 0 bits

Color

HSYNC VSYNC DATA

Range

Decoded Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

SCLK: The Clock pin.

DE: The Data Enable pin.

Hsync: The Horizontal synchronization pin.

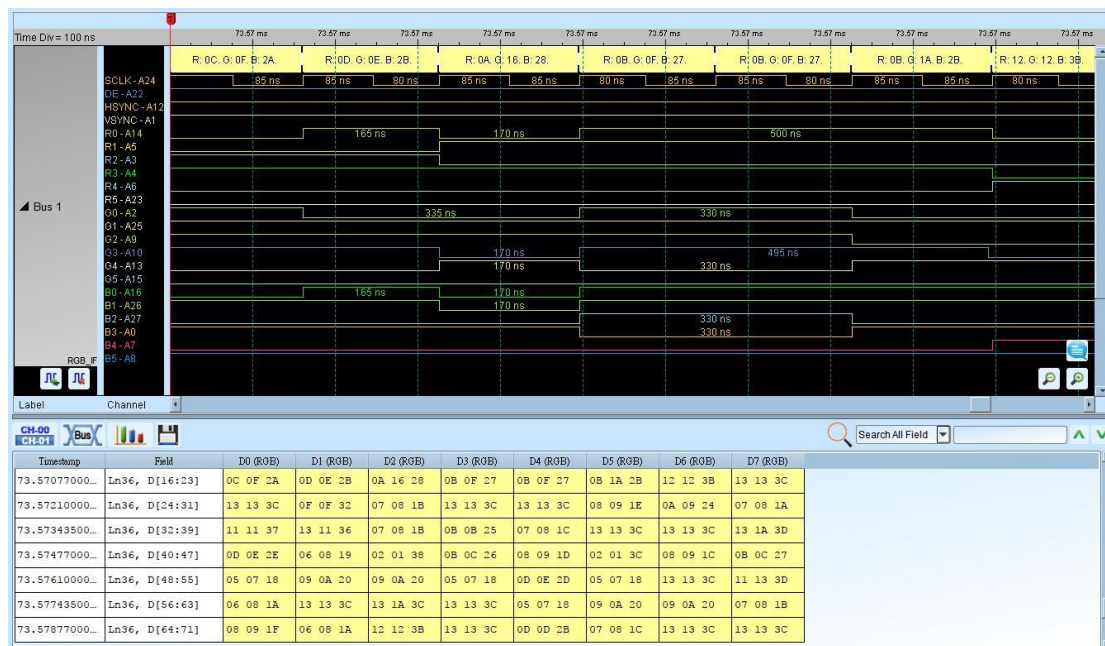
Vsync: The Vertical synchronization pin.

R0 – 7, G0 – 7, B0 – 7: RGB data pins.

Format: Select one of RGB formats or User defined.

Save as JPG file: Generate the JPG file with RGB data in the work directory of LA.

Result



S/PDIF

The Sony/Philips Digital Interconnect Format (S/PDIF) is a digital audio transmission interface with the detailed specifications below:

Data format: Default is 16 bits, up to 24 bits.

Sampling frequency:

44.1Khz from CD → Bit Rate 2.8224 Mbit/s

48 Khz from DAT → Bit Rate 3.072 Mbit/s

32 Khz from DSR → Bit Rate 2.048 Mbit/s

Deliver method: One way.

V (Validity) bit: Audio samples to confirm effectiveness, if this bit is 0, the receiver should ignore this sub-frame.

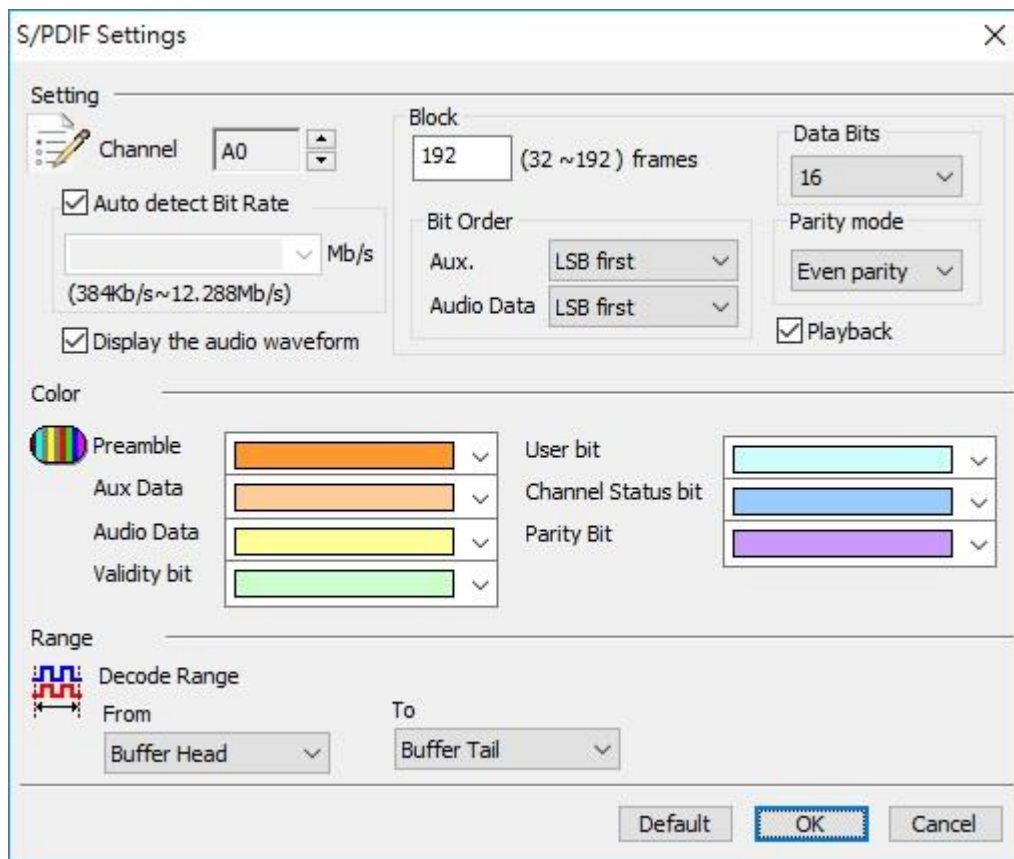
U (User) bit: User log information.

C (Channel status) bit: Channel state information.

P (Parity) bit: Parity bit check for the error.

The basic principle is to split the data bits into two parts. If the data is 1, split it into 01 or 10 or if the data is 0, split it into 00 or 11.

Settings



Channel: The default is Channel 0.

Auto detect Bit Rate: Turned on by default.

Num of frame: 192 frames within each block by default, used to analyze each sub-frame order User bit and Channel status bit.

Bit Order (Aux. Data): The default is the LSB first for the Aux. data.

Bit Order (Audio Data): The default is the LSB first for Audio data.

Data format: The default is 16 bits.

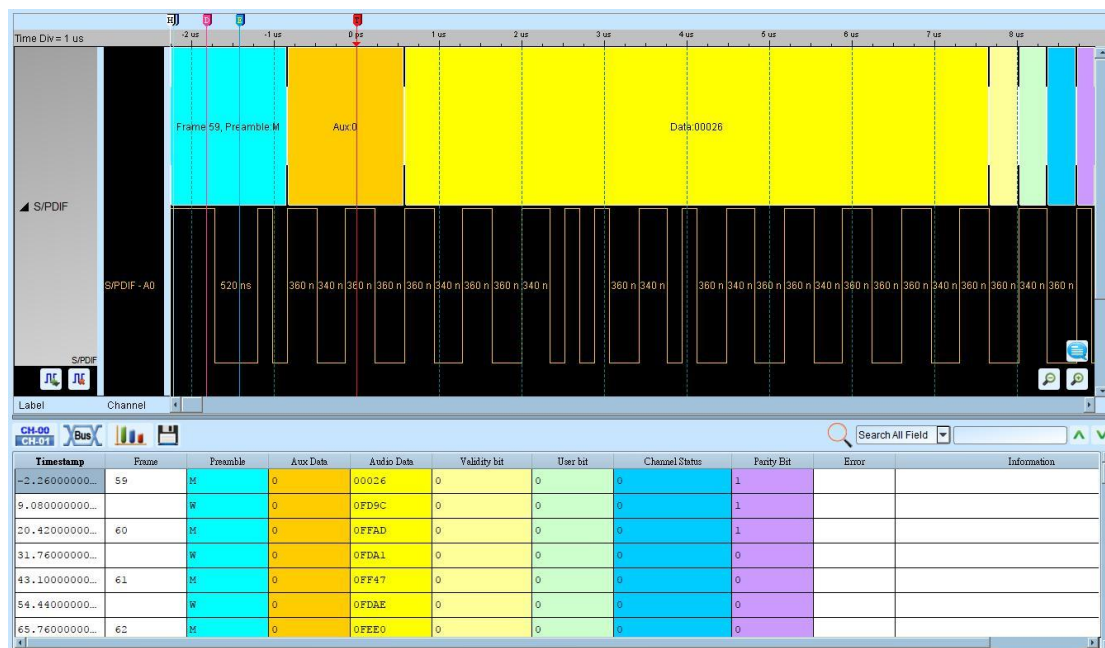
Parity mode: The default is even parity.

Display the audio waveform: Click to display the audio waveform in the Waveform Window.

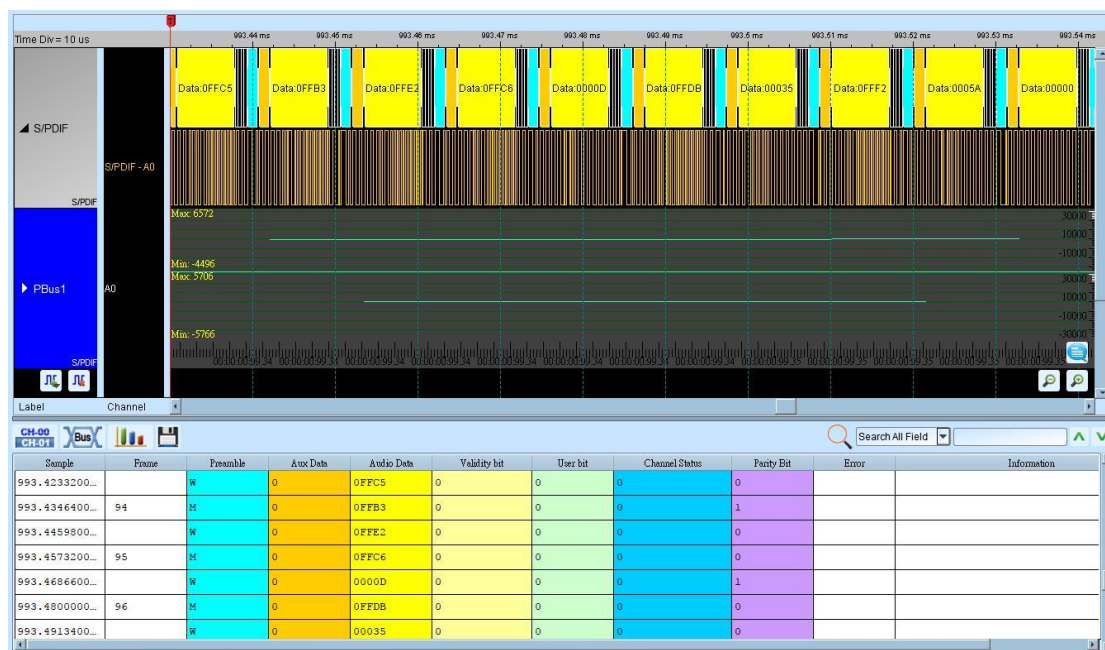
Result

Click **OK** to run the S/PDIF Decode and see the result on the Waveform Window

below.



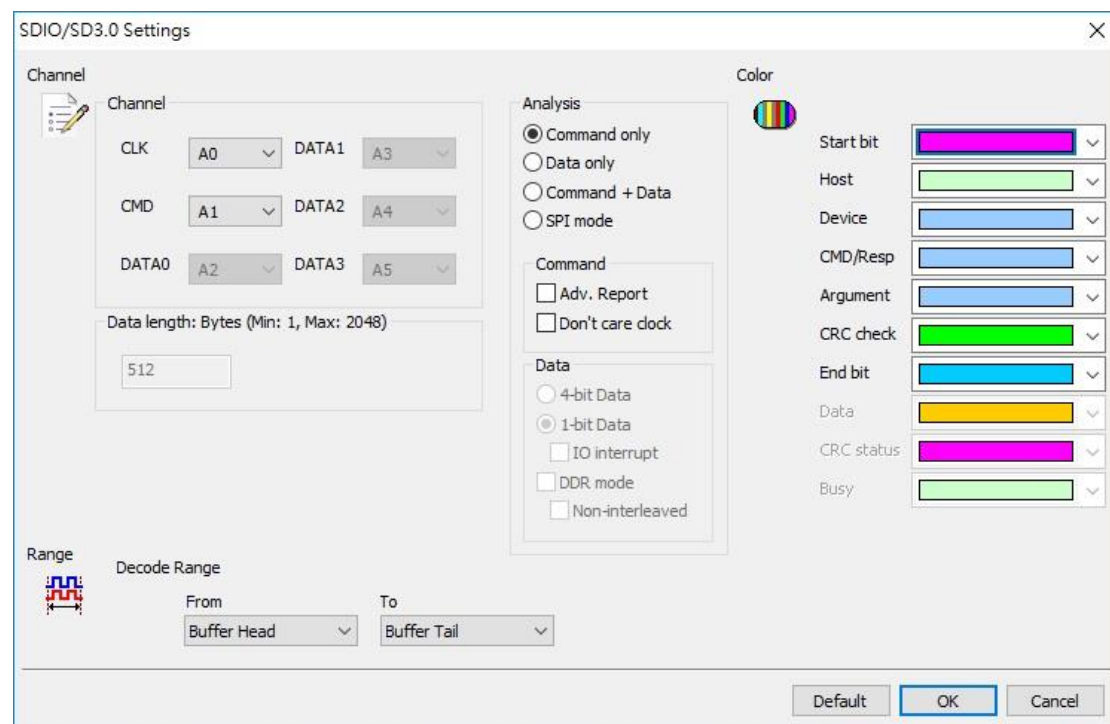
Show wave:



SDIO

The SD3.0/SDIO3.0 Protocol is a high speed serial protocol used primarily for interfacing with SD (Secure Digital) Flash memory cards.

Settings



The image shows the 'SDIO/SD3.0 Settings' dialog box. It is divided into several sections: 'Channel' with dropdowns for CLK (A0), CMD (A1), DATA0 (A2), DATA1 (A3), DATA2 (A4), and DATA3 (A5), and a 'Data length' field set to 512; 'Analysis' with radio buttons for 'Command only' (selected), 'Data only', 'Command + Data', and 'SPI mode', and checkboxes for 'Adv. Report' and 'Don't care clock'; 'Data' with radio buttons for '4-bit Data', '1-bit Data' (selected), and checkboxes for 'IO interrupt', 'DDR mode', and 'Non-interleaved'; 'Color' with a color bar and dropdowns for 'Start bit' (magenta), 'Host' (light green), 'Device' (light blue), 'CMD/Resp' (light blue), 'Argument' (light blue), 'CRC check' (green), 'End bit' (cyan), 'Data' (yellow), 'CRC status' (magenta), and 'Busy' (light green); and 'Range' with a 'Decode Range' section showing 'From' (Buffer Head) and 'To' (Buffer Tail). At the bottom are 'Default', 'OK', and 'Cancel' buttons.

Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data.

Command + Data: Analyze Command and Data in the report window.

Adv. Report: Analyze the command argument

Don't care clock: decode only depend on the CMD channel.

Data: 1/4/8 bits or DDR mode, check "IO interrupt" when SDIO 1 bit mode and support the IO interrupt decode via DATA1 channel, check "DDR mode" and "Non-interleaved" to analyze data without interleaved.

Data length: Set the length of data.

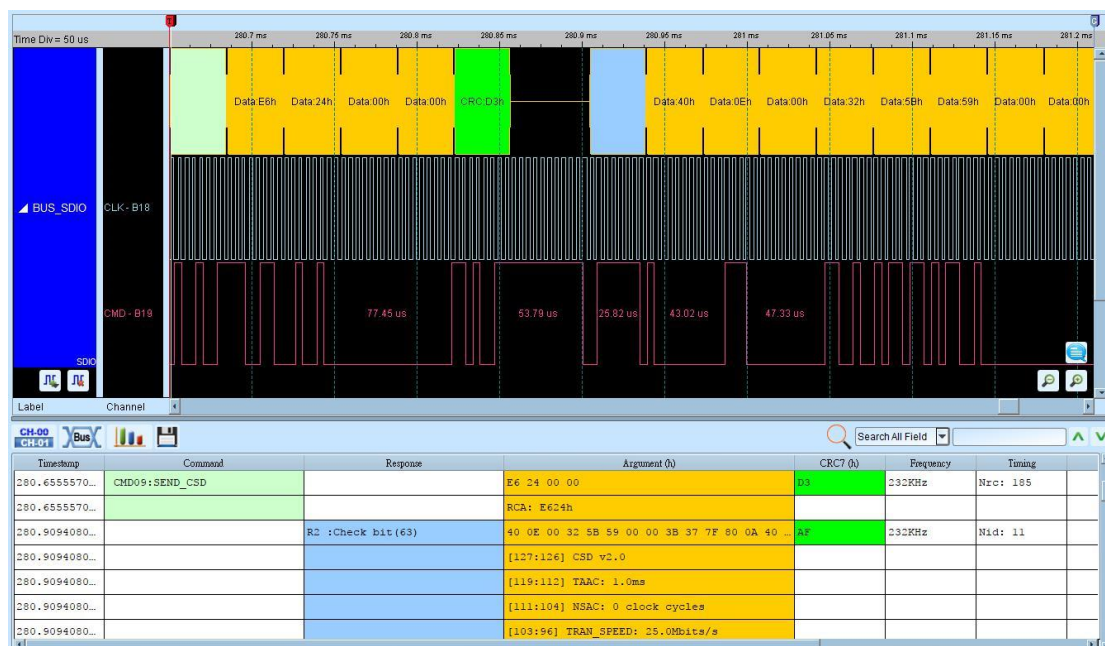
Result

Click **OK** to run the SDI/O decode and see the result on the Waveform Window below.

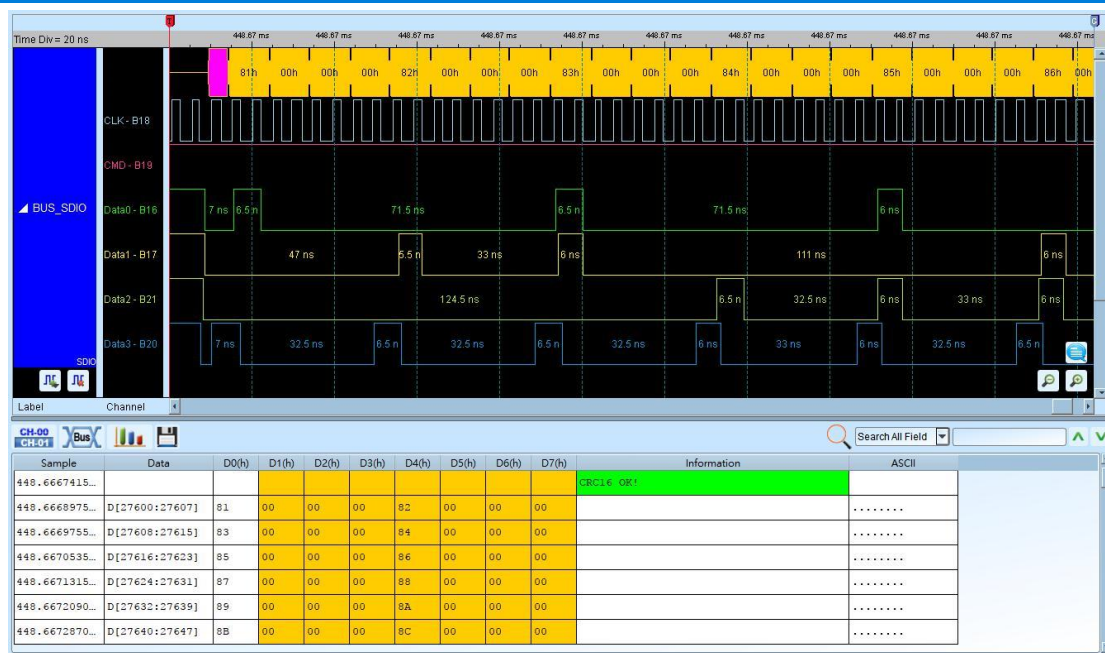
CMD mode



Adv. Report



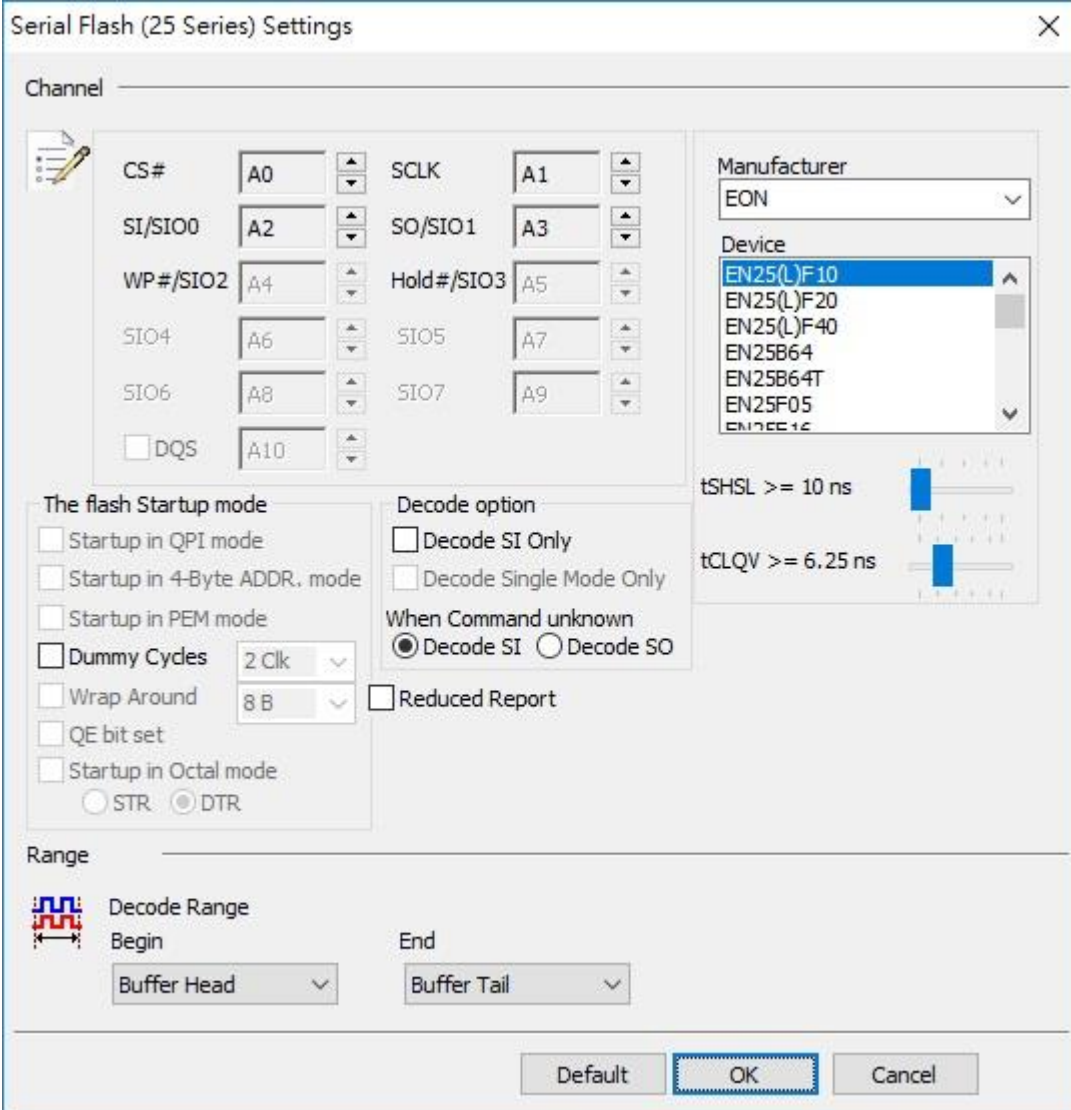
Data mode



Serial Flash

SPI Serial Flash is small, low-power flash memory that features Serial Peripheral Interface (SPI) and pin-for-pin compatibility with industry-standard SPI EEPROM devices.

Settings



The image shows the 'Serial Flash (25 Series) Settings' dialog box. It is divided into several sections:

- Channel:** A list of pins with dropdown menus for configuration. The pins are CS#, SI/SIO0, WP#/SIO2, SIO4, SIO6, DQS, SCLK, SO/SIO1, Hold#/SIO3, SIO5, SIO7, and A10. The dropdowns show values like A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, and A10.
- Manufacturer:** A dropdown menu showing 'EON'.
- Device:** A list box showing various device models: EN25(L)F10, EN25(L)F20, EN25(L)F40, EN25B64, EN25B64T, EN25F05, and EN25F16. 'EN25(L)F10' is selected.
- tSHSL >= 10 ns:** A slider control for setting the tSHSL value.
- tCLQV >= 6.25 ns:** A slider control for setting the tCLQV value.
- The flash Startup mode:** A group of checkboxes and a dropdown menu. Options include 'Startup in QPI mode', 'Startup in 4-Byte ADDR. mode', 'Startup in PEM mode', 'Dummy Cycles' (set to 2 Clk), 'Wrap Around' (set to 8 B), 'QE bit set', and 'Startup in Octal mode'. The 'STR' radio button is selected.
- Decode option:** A group of checkboxes and radio buttons. Options include 'Decode SI Only', 'Decode Single Mode Only', and 'When Command unknown' (with 'Decode SI' selected).
- Reduced Report:** A checkbox.
- Range:** A section with a 'Decode Range' icon, 'Begin' and 'End' dropdown menus (set to 'Buffer Head' and 'Buffer Tail' respectively), and a 'Range' label.
- Buttons:** 'Default', 'OK', and 'Cancel' buttons at the bottom.

Channel: Show the selected channels (CH0 – CH5).

Manufacturer/Device: Select the Serial Flash device type, tCLQV and tSHSL.

QPI mode: Quad Peripheral Interface Mode/Quad SPI Mode

4-Byte mode: 4-Byte Address Mode

PEM mode: Performance Enhance Mode

Dummy Cycles: Clock buffers between read command and data.

Wrap Around: Wrap number

QE bit: Enable or disable the QPI mode.

Decode SI Only: Single mode, 3-wire → CS#, SCLK, SI.

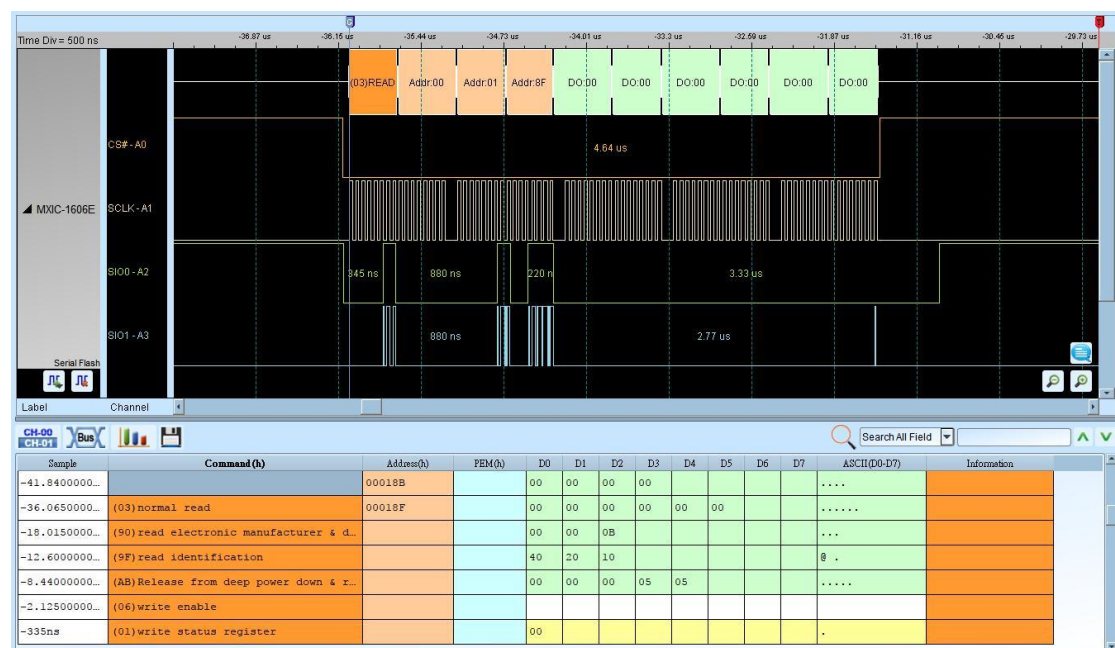
Decode Single Mode Only: Single mode, 4-wire → CS, Clock, SI, SO.

The LA viewer will choose 4-wire or 6-wire to analyze according to the Serial Flash device type.

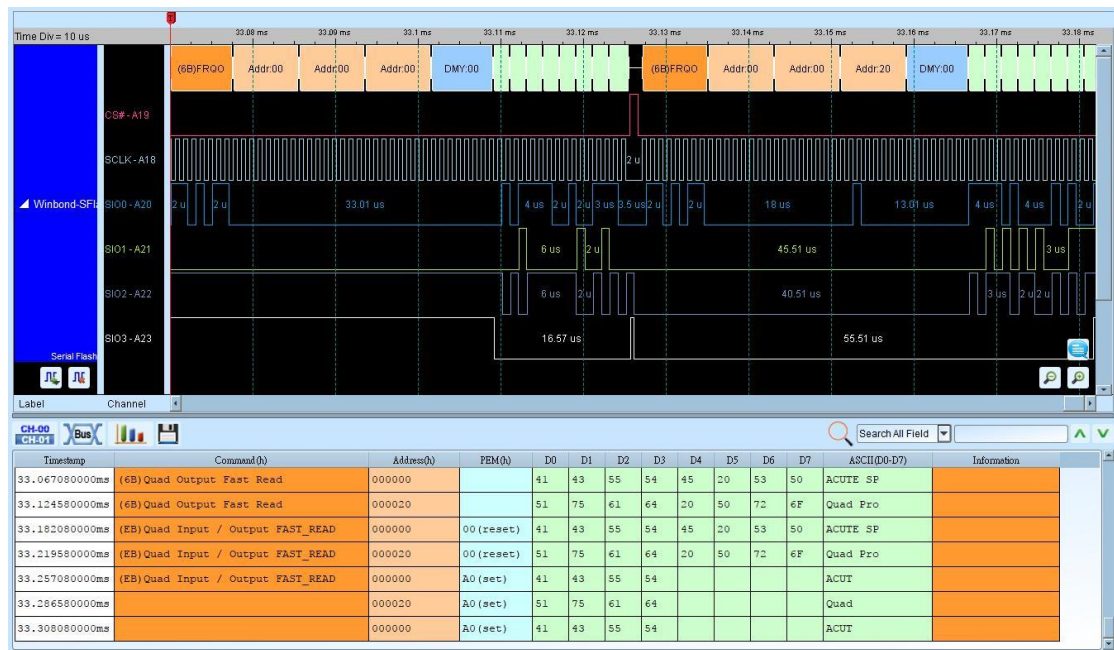
Result

Click **OK** to run the Serial Flash decode and see the result on the Waveform Window below.

Serial Flash decode within SPI mode.

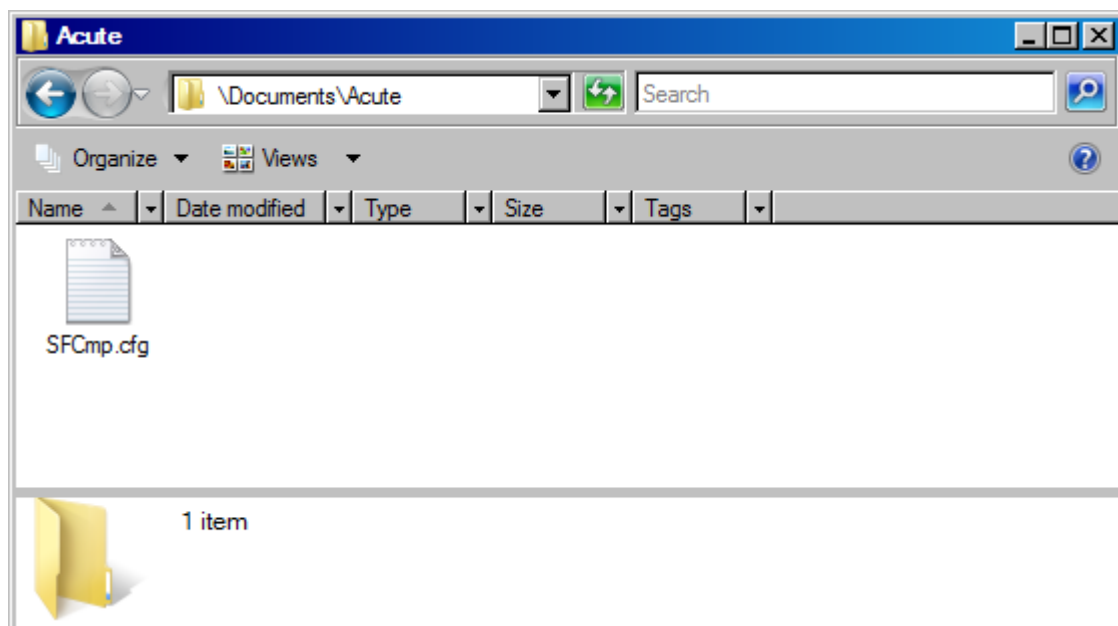


Serial Flash decode within QPI mode.

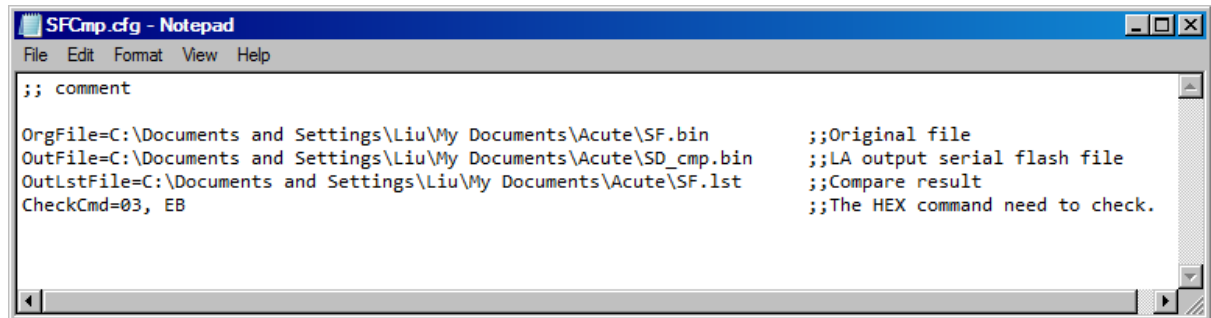


Serial Flash data Comparison : Compare the Serial Flash data by the waveform files.

Method: Create a file by text editor and save it as SFCmp.cfg in order to compare with the real Serial Flash waveform to find the bug, the default path is “My Documents\Acute”



SFCmp.cfg information:



```
;; comment

OrgFile=C:\Documents and Settings\Liu\My Documents\Acute\SF.bin      ;;Original file
OutFile=C:\Documents and Settings\Liu\My Documents\Acute\SD_cmp.bin  ;;LA output serial flash file
OutLstFile=C:\Documents and Settings\Liu\My Documents\Acute\SF.lst   ;;Compare result
CheckCmd=03, EB              ;;The HEX command need to check.
```

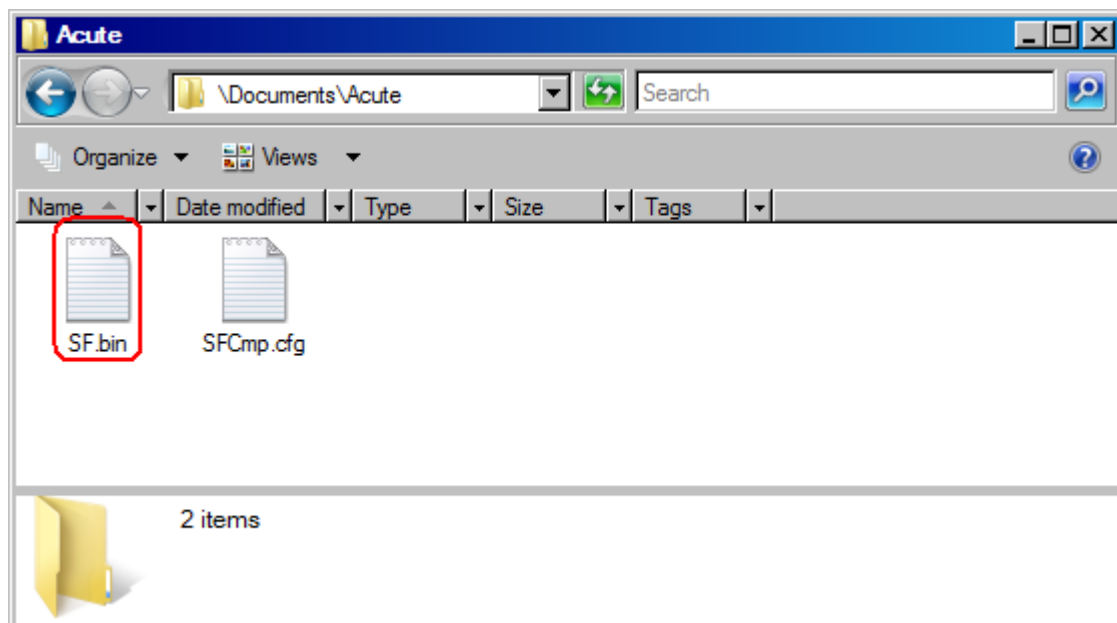
OrgFile=File_Path: Key in the file path of the original Serial Flash data file (.bin).

OutFile=File_Path: Key in the file path of the Serial Flash output file.

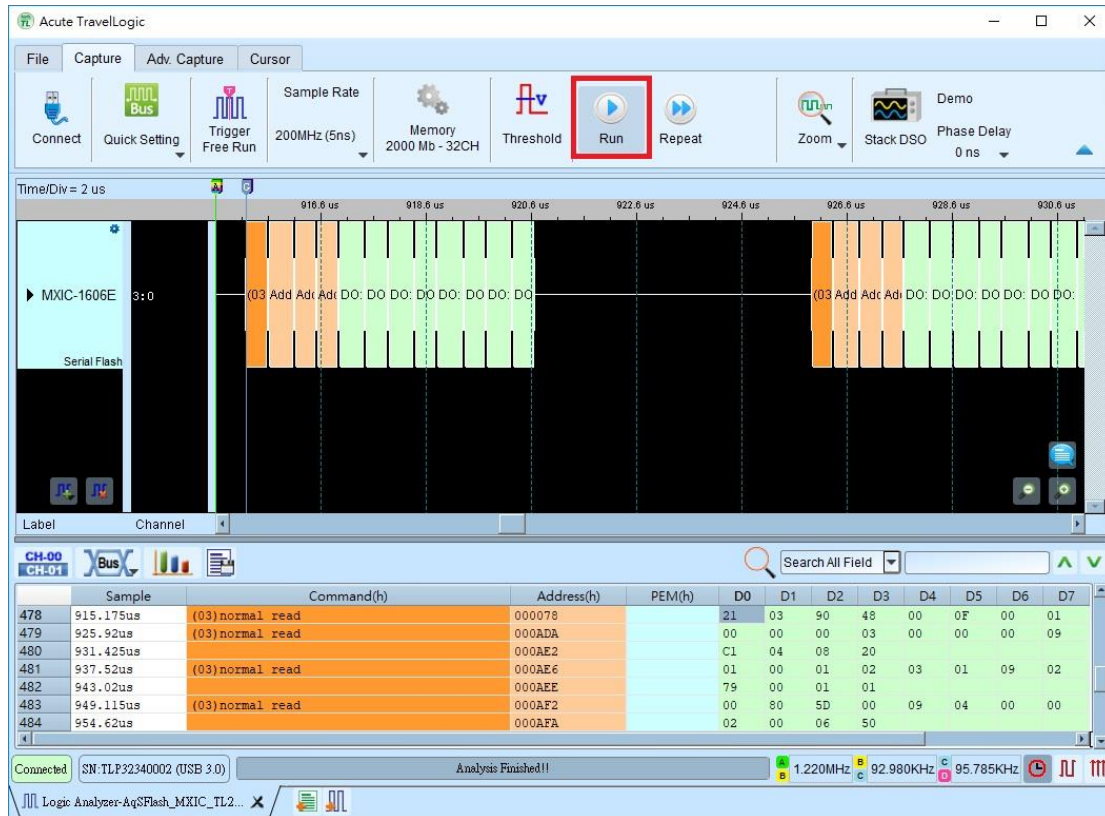
OutLstFile=File_Path: Key in the file path of the comparison result. The file name will has extension “.lst”.

CheckCmd=Serial Flash command: Key in the command in Hex that are separated by commas.

Save the OrgFile to the OrgFile file path.

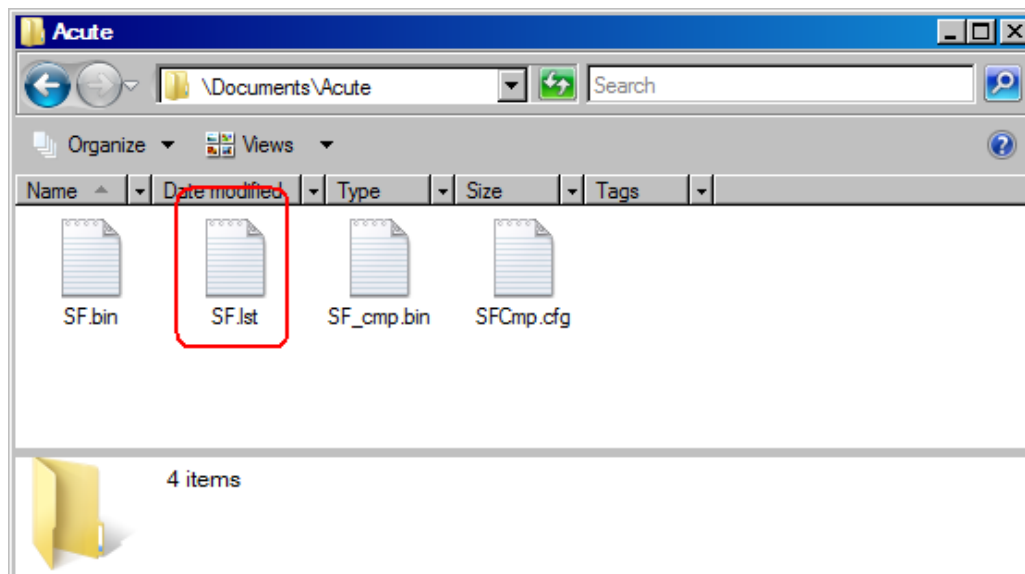


Run the Serial Flash Bus Decode to capture the Serial Flash signal.

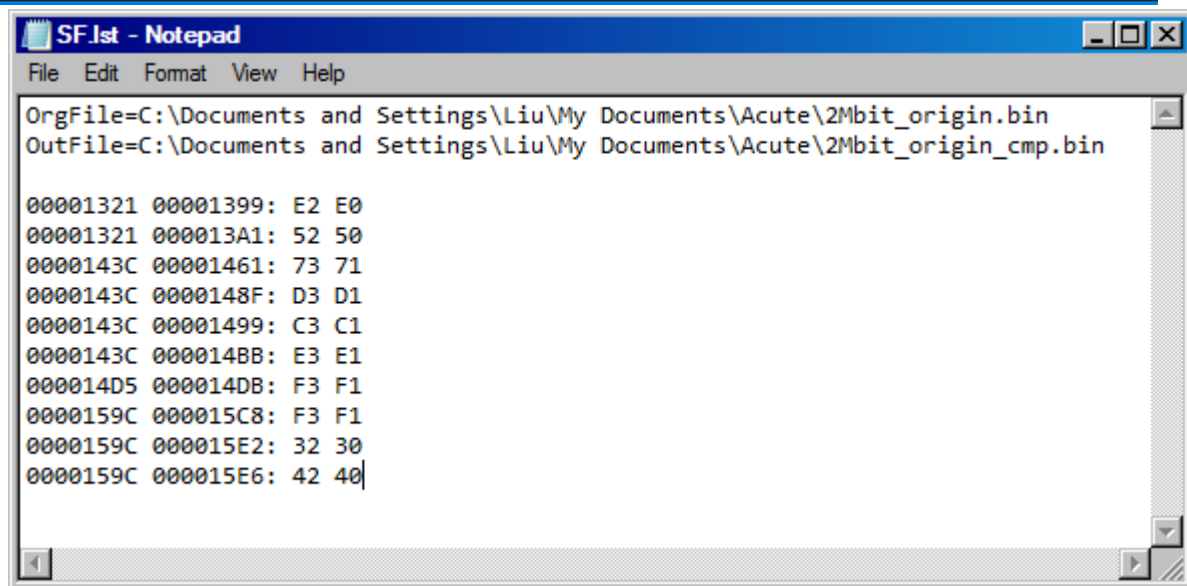


If the OutFile does not exist, it will copy the OrgFile to the OutFile and write the data to it according to the CheckCmd.

Compare result:



The OutLstFile:



```
SF.lst - Notepad
File Edit Format View Help
OrgFile=C:\Documents and Settings\Liu\My Documents\Acute\2Mbit_origin.bin
OutFile=C:\Documents and Settings\Liu\My Documents\Acute\2Mbit_origin_cmp.bin

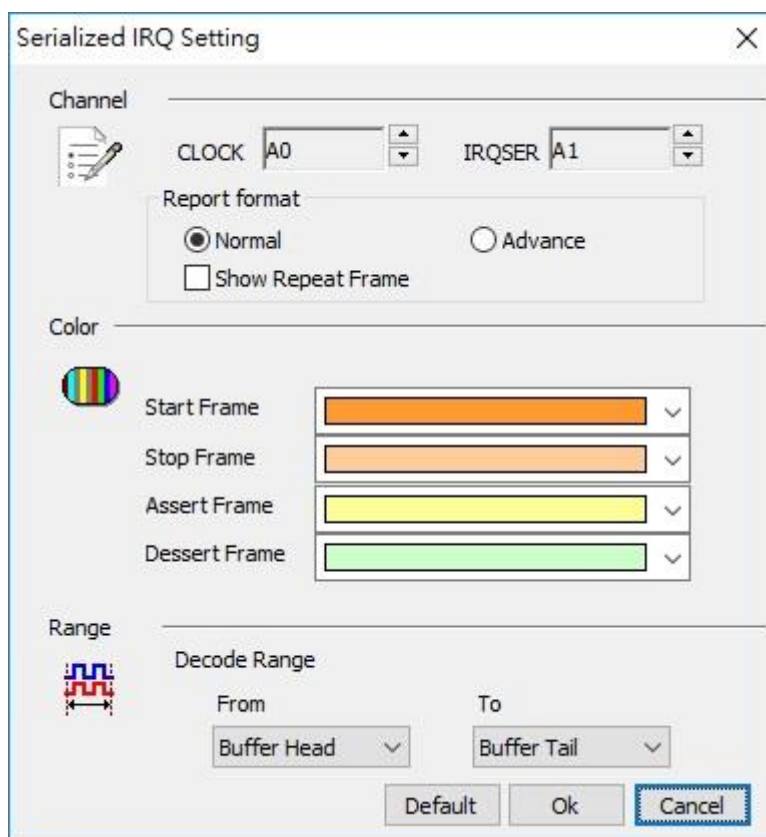
00001321 00001399: E2 E0
00001321 000013A1: 52 50
0000143C 00001461: 73 71
0000143C 0000148F: D3 D1
0000143C 00001499: C3 C1
0000143C 0000148B: E3 E1
000014D5 000014DB: F3 F1
0000159C 000015C8: F3 F1
0000159C 000015E2: 32 30
0000159C 000015E6: 42 40
```

The first column is the compared address from OrgFile, the second column is the different address from OutFile.

Serial IRQ

The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device's IRQ(s) and/or Data to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame. This protocol uses the PCI Clock as its clock source and conforms to the PCI bus electrical specification.

Settings



The image shows a 'Serialized IRQ Setting' dialog box. It has a title bar with a close button. The dialog is divided into several sections: 'Channel' with 'CLOCK' and 'IRQSER' dropdown menus; 'Report format' with 'Normal' (selected) and 'Advance' radio buttons, and a 'Show Repeat Frame' checkbox; 'Color' with a color palette icon and four color-coded frame type selectors (Start Frame, Stop Frame, Assert Frame, Dessert Frame); and 'Range' with a range icon and 'Decode Range' dropdowns for 'From' and 'To'. At the bottom are 'Default', 'Ok', and 'Cancel' buttons.

Serialized IRQ Setting

Channel

CLOCK A0 IRQSER A1

Report format

☒ Normal ☐ Advance

☐ Show Repeat Frame

Color

Start Frame

Stop Frame

Assert Frame

Dessert Frame

Range

Decode Range

From Buffer Head To Buffer Tail

Default Ok Cancel

CLOCK: PCI Clock channel

IRQSER; IRQSER channel

Normal: Not show repeat frame

Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10286946	22830	Continue mode		A					A						A				
10291906	22841	Continue mode		A					A						A				
10404663	23091	Continue mode		A					A						A				
10415039	23114	Continue mode		A											A				
10459240	23212	Continue mode		A					A						A				
10461943	23218	Continue mode		A											A				
10580112	23480	Continue mode		A					A						A				
10590037	23502	Continue mode		A											A				
10634238	23600	Continue mode		A					A						A				
10636941	23606	Continue mode		A											A				

Show repeat frame

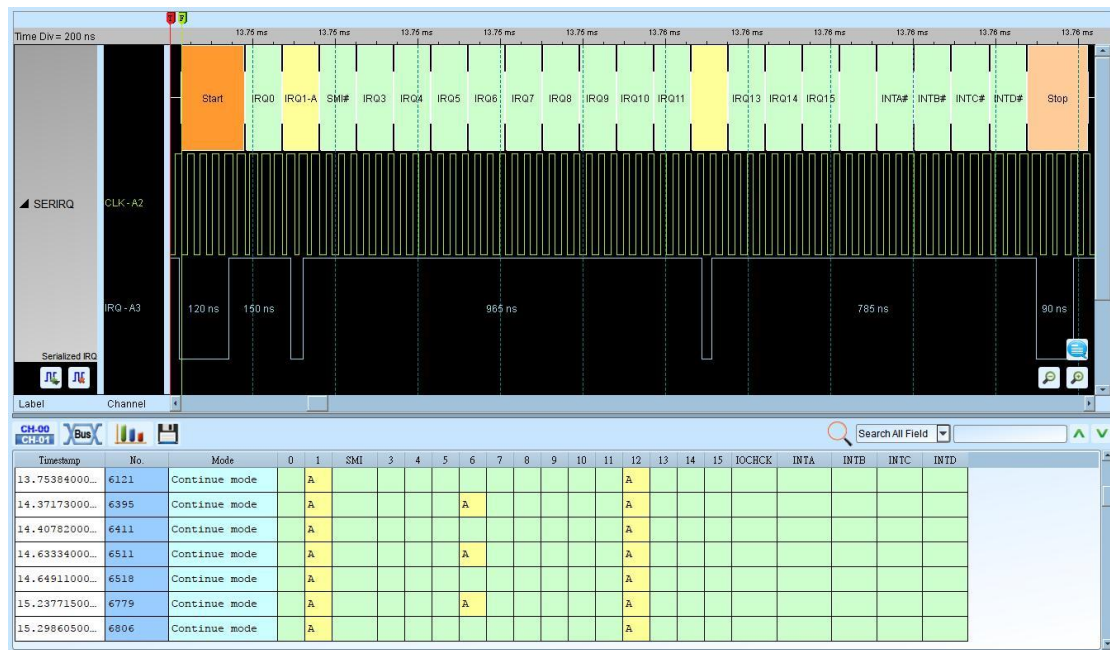
Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10457887	23209	Continue mode		A											A				
10458338	23210	Continue mode		A											A				
10458789	23211	Continue mode		A											A				
10459240	23212	Continue mode		A					A						A				
10459690	23213	Continue mode		A					A						A				
10460140	23214	Continue mode		A					A						A				
10460590	23215	Continue mode		A					A						A				
10461041	23216	Continue mode		A					A						A				
10461492	23217	Continue mode		A					A						A				
10461943	23218	Continue mode		A											A				
10462394	23219	Continue mode		A											A				
10462846	23220	Continue mode		A											A				
10463298	23221	Continue mode		A											A				

Advance:

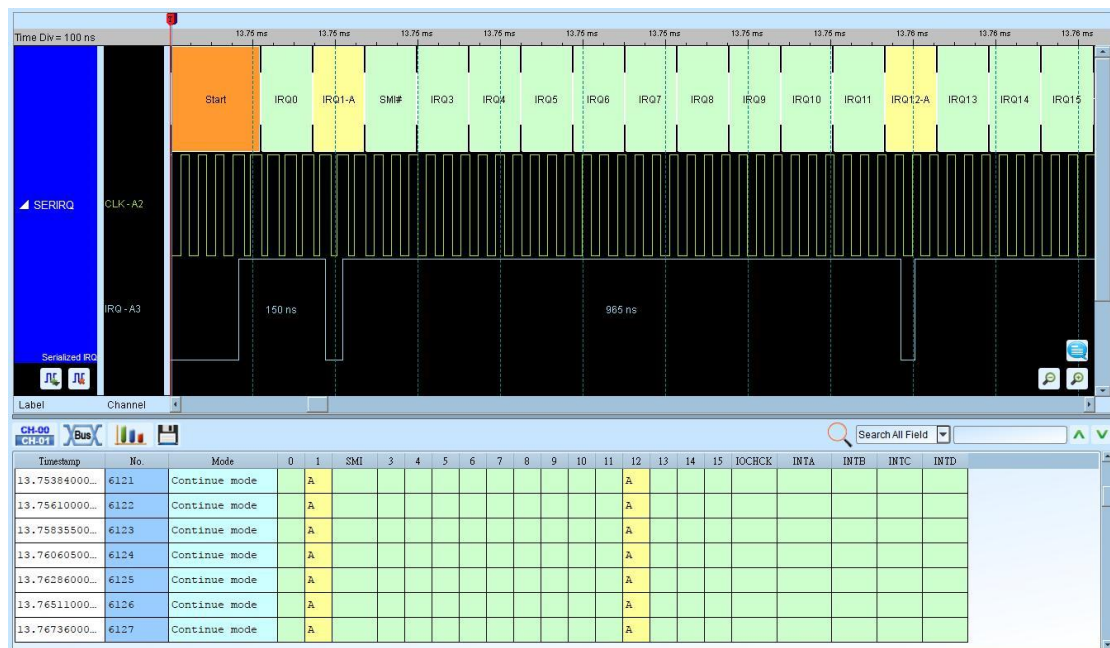
Clock	IRQ/Data Frame	Signal Sampled	# of clocks past Start
-9470	1	IRQ0	2
-9452	2	IRQ1	5
-9434	3	SMI#	8
-9416	4	IRQ3	11
-9398	5	IRQ4	14
-9380	6	IRQ5	17
-9362	7	IRQ6	20
-9344	8	IRQ7	23
-9326	9	IRQ8	26
-9308	10	IRQ9	29
-9290	11	IRQ10	32
-9272	12	IRQ11	35
-9254	13	IRQ12	38
-9236	14	IRQ13	41
-9217	15	IRQ14	44
-9199	16	IRQ15	47
-9181	17	IOCHCK#	50
-9163	18	INTA#	53
-9145	19	INTB#	56
-9127	20	INTC#	59
-9109	21	INTD#	62
-9019	1	IRQ0	2
-9001	2	IRQ1	5

Result

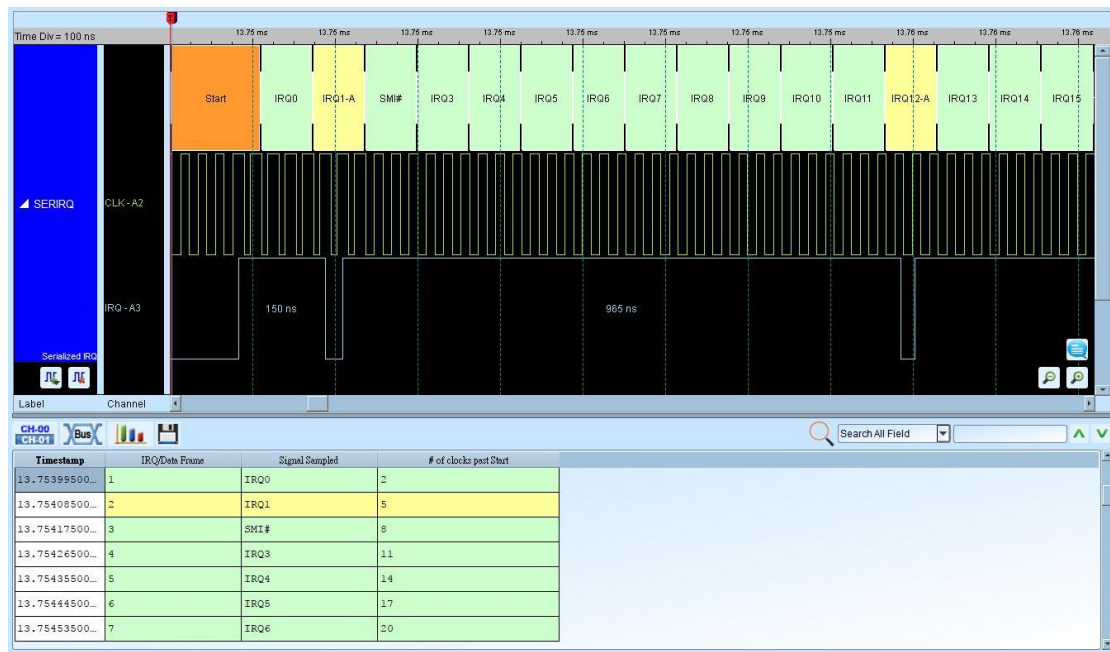
Normal mode



Normal mode(Show repeat frame)



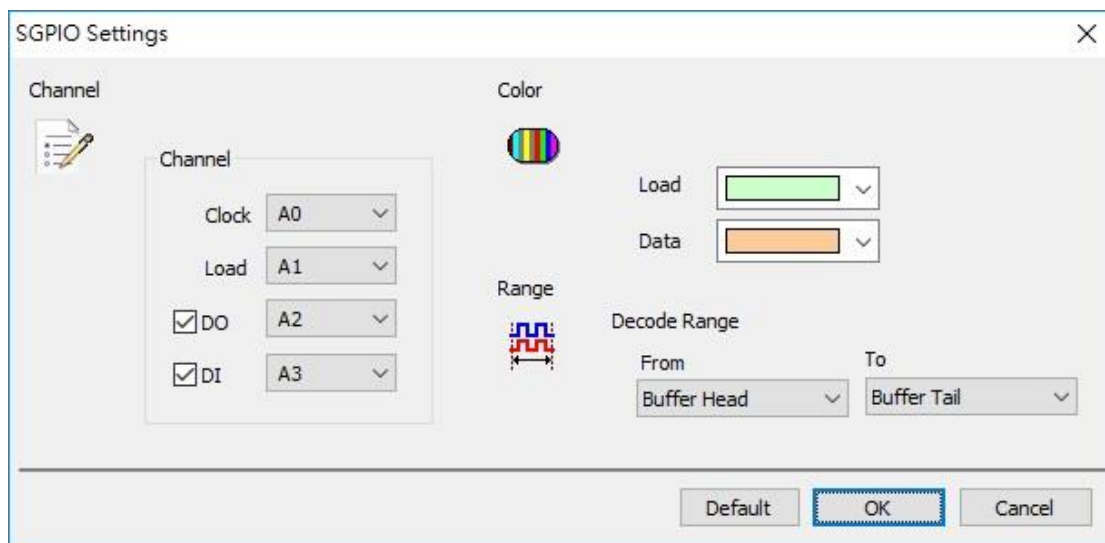
Advance mode



Serial General Purpose Input Output (SGPIO)

The SGPIO is a method to serialize general purpose IO signals. SGPIO defines the communication between an initiator and a target.

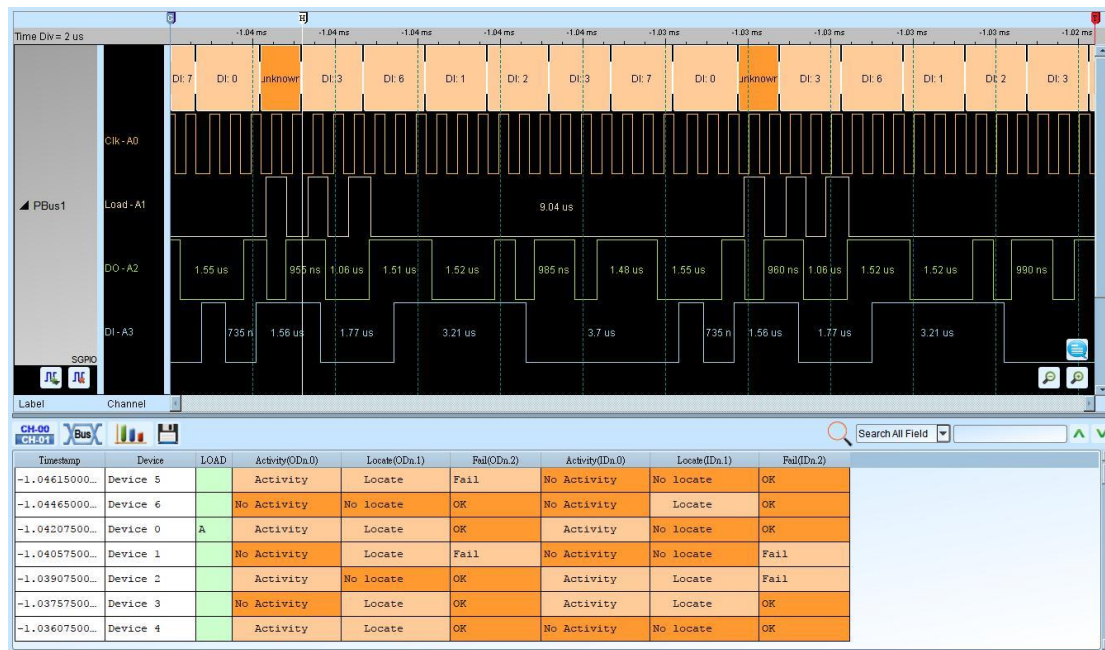
Settings



Channel: Show the selected channels (Clock, Load and Data), it can only use data out or date in or both.

Result:

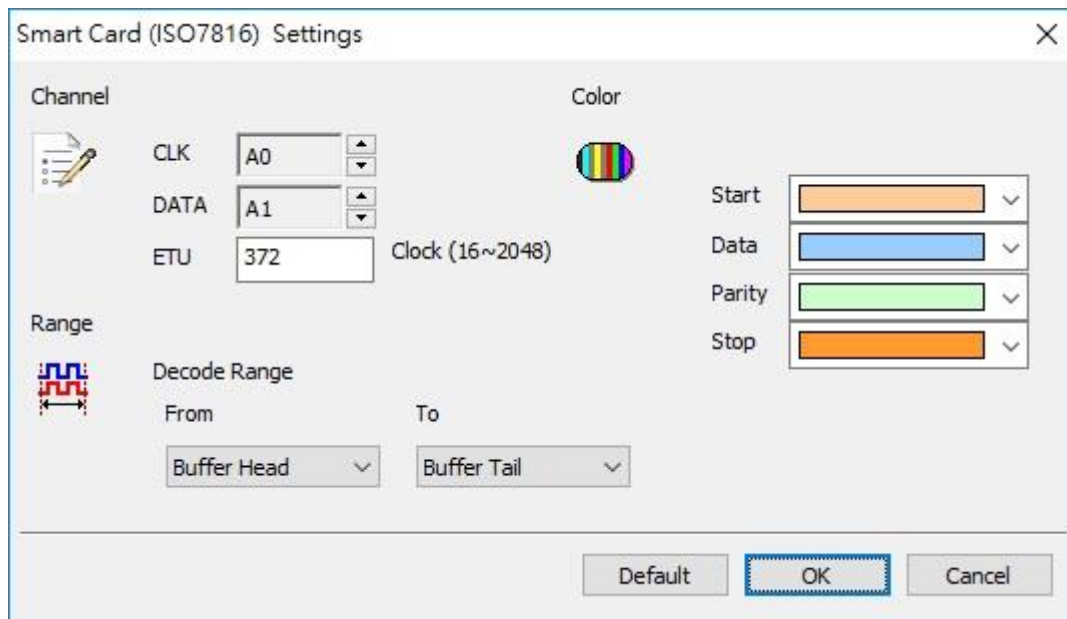
Click OK to run the Smart Card decode and see the result on the Waveform Window below.



Smart Card (ISO7816)

The card is made of plastic and provides strong security authentication for single sign-on within large organizations.

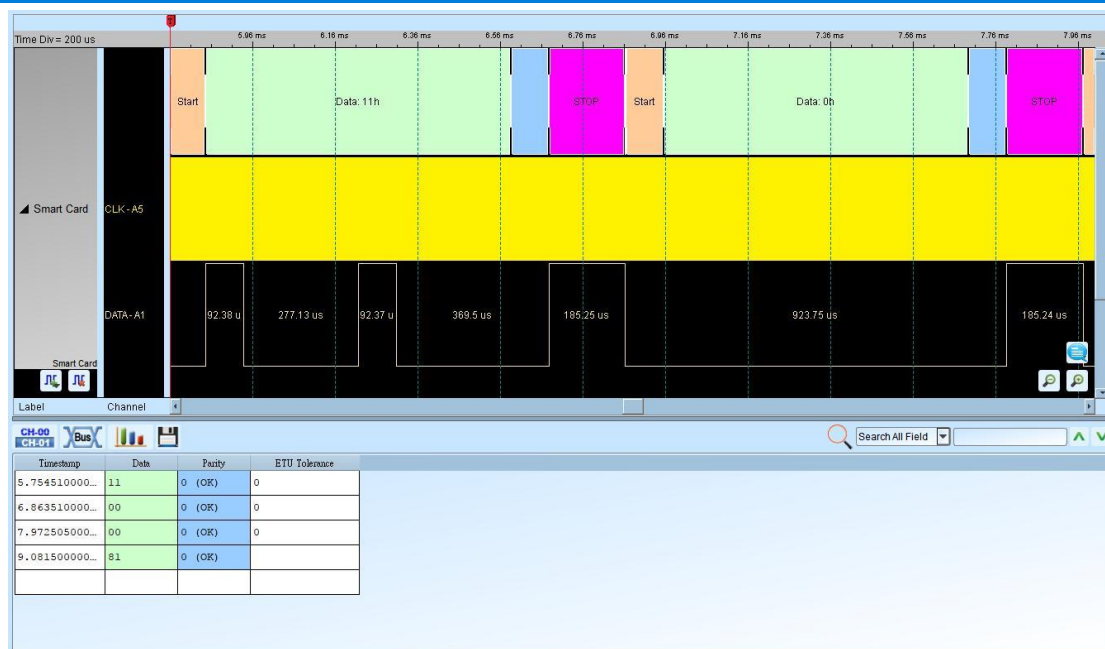
Settings



Channel: Show the selected channels (CLK and DATA) and the number of clocks within the bit (ETU).

Result

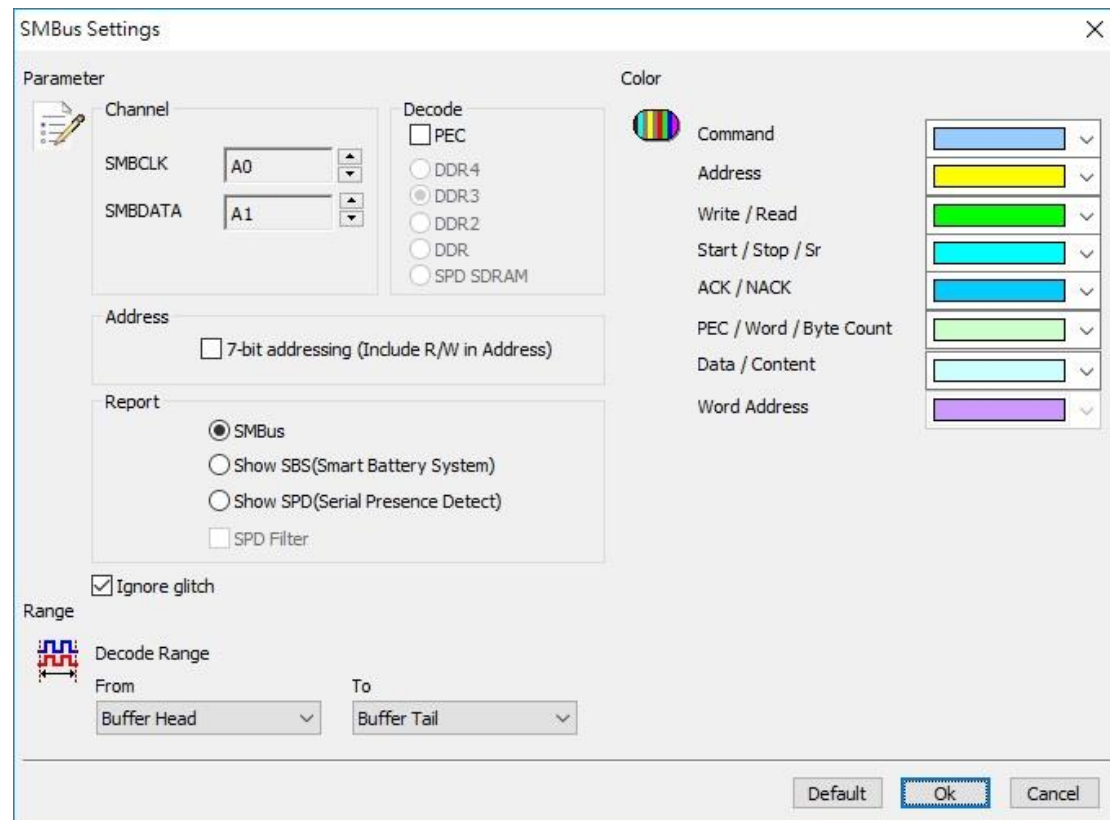
Click **OK** to run the Smart Card decode and see the result on the Waveform Window below.



System Management Bus (SMBus)

The SMBus (SMB) is a two-wire bus.

Settings



The image shows the 'SMBus Settings' dialog box. It is divided into several sections: 'Parameter' on the left, 'Decode' in the middle, 'Color' on the right, and 'Range' at the bottom. The 'Parameter' section includes 'Channel' with 'SMBCLK' set to 'A0' and 'SMBDATA' set to 'A1', an 'Address' section with a checkbox for '7-bit addressing (Include R/W in Address)', a 'Report' section with radio buttons for 'SMBus', 'Show SBS(Smart Battery System)', and 'Show SPD(Serial Presence Detect)', and a checkbox for 'SPD Filter'. The 'Decode' section has a 'Decode' checkbox and radio buttons for 'DDR.4', 'DDR.3', 'DDR.2', 'DDR', and 'SPD SDRAM'. The 'Color' section has a 'Color' icon and a list of color-coded items: 'Command' (blue), 'Address' (yellow), 'Write / Read' (green), 'Start / Stop / Sr' (cyan), 'ACK / NACK' (light blue), 'PEC / Word / Byte Count' (light green), 'Data / Content' (light cyan), and 'Word Address' (purple). The 'Range' section has a 'Range' icon, a 'Decode Range' checkbox, and 'From' and 'To' dropdown menus set to 'Buffer Head' and 'Buffer Tail' respectively. At the bottom are 'Default', 'Ok', and 'Cancel' buttons.

Clock: Show the selected channels (SMBCLK CH0 and SMBDATA CH1).

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

Show SBS (Smart Battery System): Show the Smart Battery System: voltage, electric current and the manufacturer.

Show SPD(Serial Presence Detect) : Report window show the configuration of memory module(DDR3, DDR2, DDR, SPD SDRAM) in EEPROM.

SBS/SPD Filter: Report window only show SBS/SPD packet.

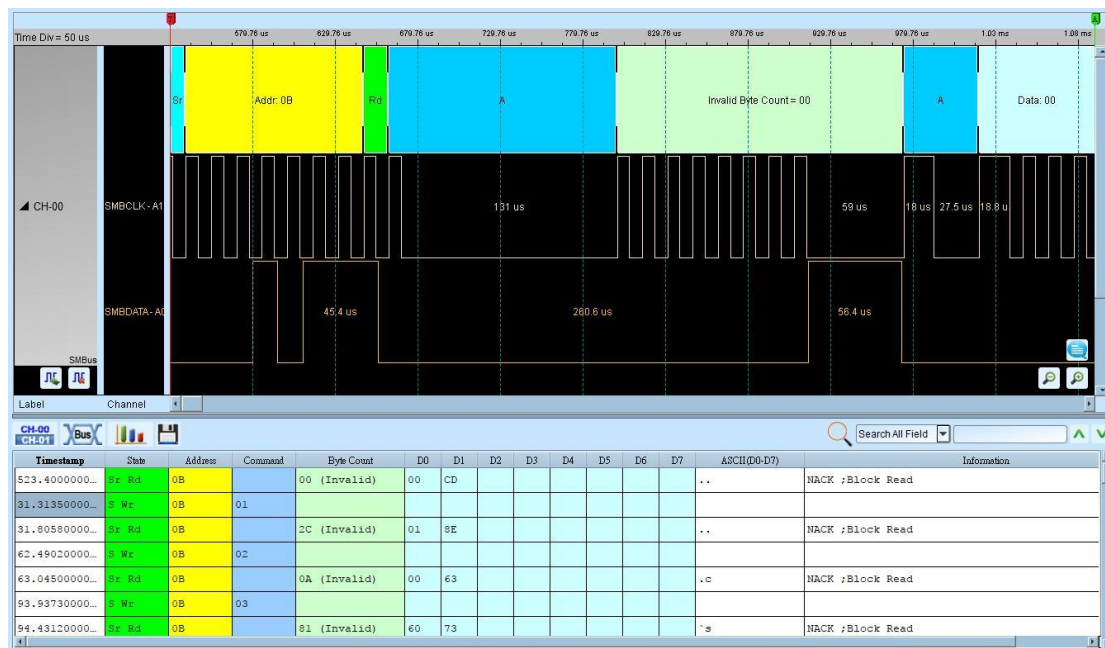
Ignore glitch: Ignore the glitch when the slow transitions.

Result

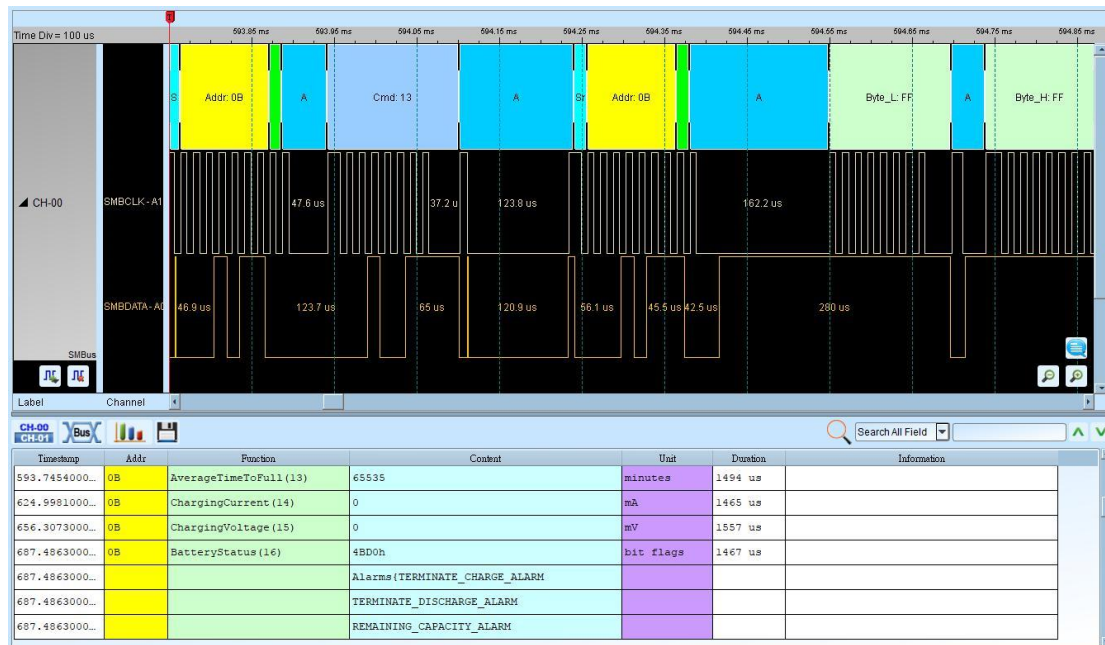
Click **OK** to run the SMBus Decode and see the result on the Waveform Window

below.

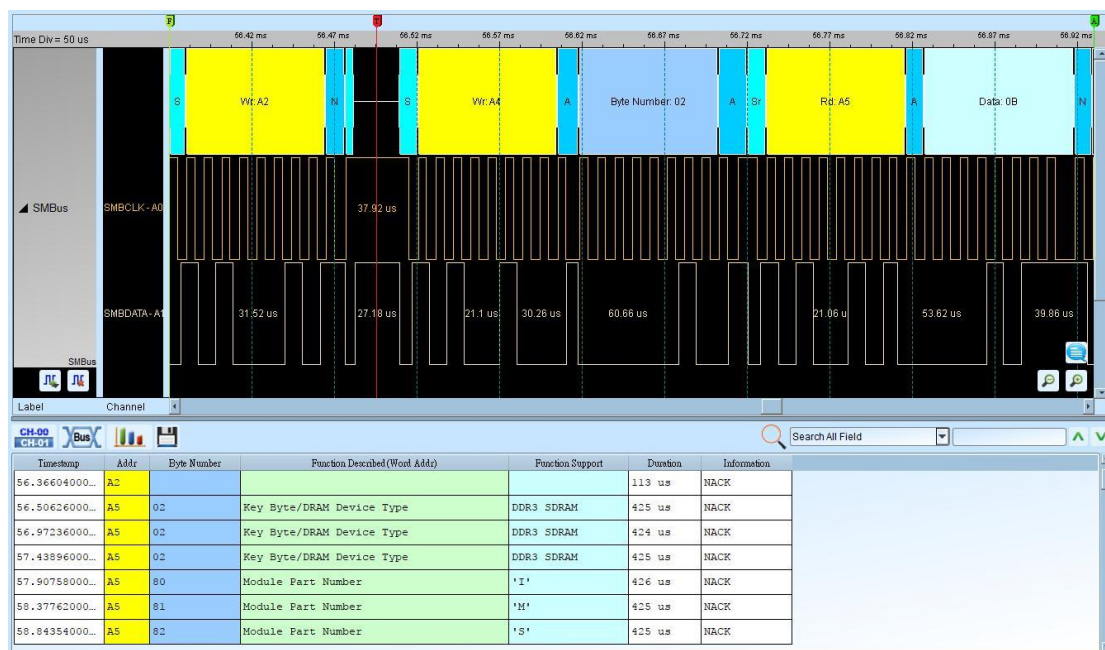
SMBus



Show SBS (Smart Battery System)



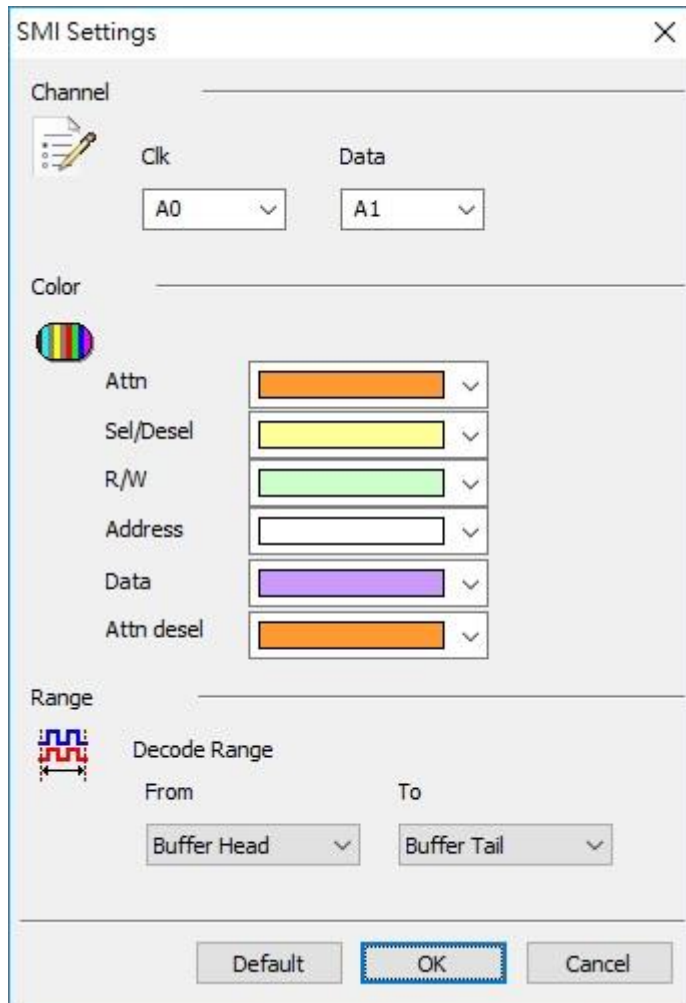
Show SPD (Serial Presence Detect)



Serial Microprocessor Interface (SMI)

The SMI is a two-wire bus.

Settings

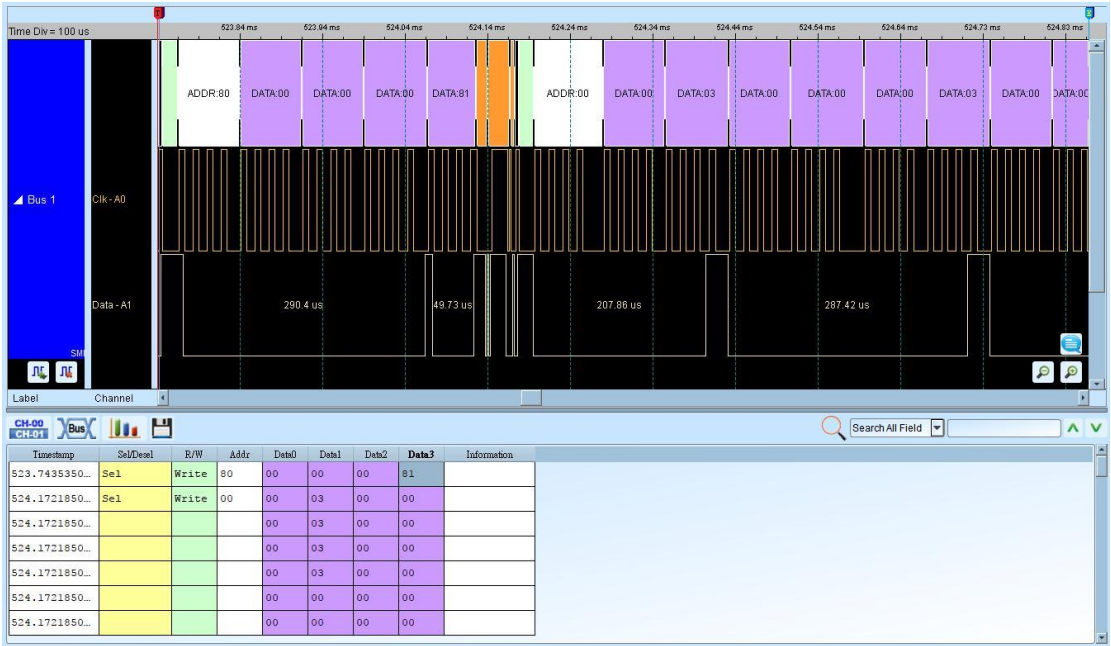


The SMI Settings dialog box is divided into three sections: Channel, Color, and Range. The Channel section has a list icon and two dropdown menus for Clk (A0) and Data (A1). The Color section has a color wheel icon and six color selection boxes with dropdown arrows for Attn (orange), Sel/Desel (yellow), R/W (light green), Address (white), Data (purple), and Attn desel (orange). The Range section has a waveform icon and a Decode Range section with From (Buffer Head) and To (Buffer Tail) dropdown menus. At the bottom are Default, OK, and Cancel buttons.

Section	Item	Value
Channel	Clk	A0
	Data	A1
Color	Attn	Orange
	Sel/Desel	Yellow
	R/W	Light Green
	Address	White
	Data	Purple
	Attn desel	Orange
Range	From	Buffer Head
	To	Buffer Tail

Channel: Show the selected channels (Clk and Data)

Result



Serial Peripheral Interface (SPI)

The SPI, is one kind of 4-wires synchronous serial data link. The SPI bus can be 4 wires, 3 wires, or 2 wires.

Settings

Type: The default is 3 Wire-SPI.

SPI Settings

Setting

Type
3 Wire-SPI

☐ Use External clock

Clock Channel(SCK) A1

Bit Order MSB First

Word Size 8 bit (4~40)

Data valid from SCK 0 S/R Clk

Report

☒ Show Idle state in report window

☐ Reduce report

Show data in report 16 Column

3 Wire-SPI

Chip Select Channel (CS) A0

Data Channel (SDA) A2

Chip Select Edge Active Low

Data Edge Rising

☐ SDI(Write)-Latency-SDO(Read)

Write Length 0 Latency 2

Read Length 32776 (Bits)

Color

SDI/SDA/Write Channel

SDO/Read Channel

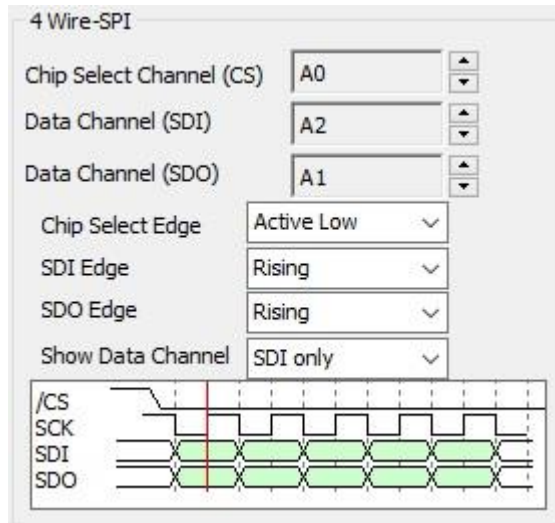
Range

Decode Range

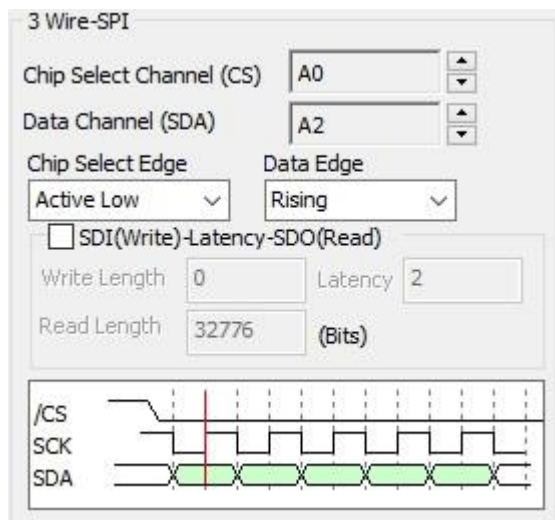
From Buffer Head To Buffer Tail

Default OK Cancel

4 Wire-SPI dialog box → CS, SCK, SDI, SDO

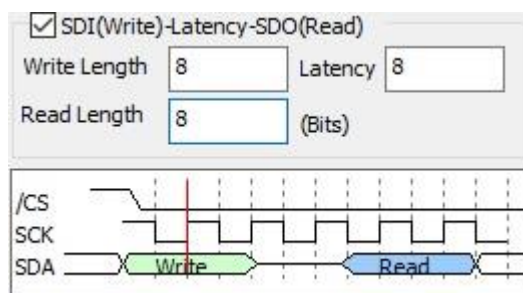


3 Wire-SPI dialog box → CS, SCK, SDA

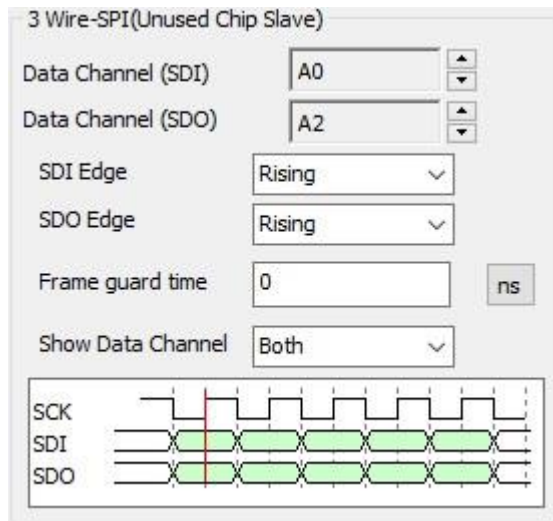


Click the SDI(Write)-Latency-SDO(Read) to show the dialog below.

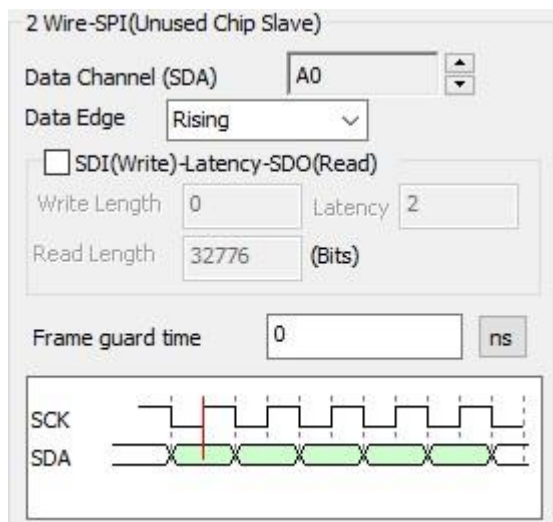
The maximum length is 65535 (Bits)



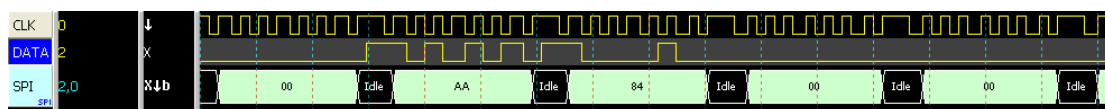
3 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDI, SDO

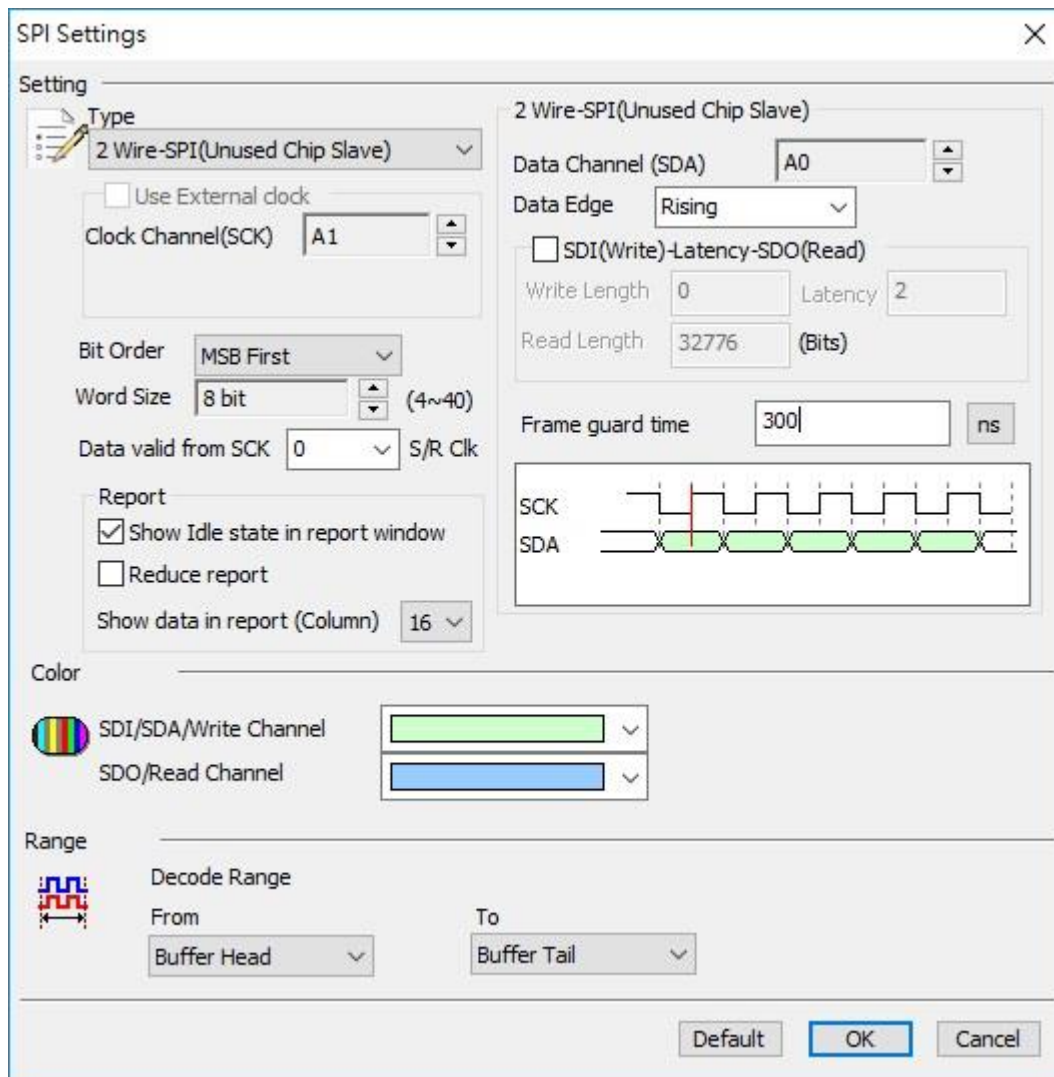


2 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDA

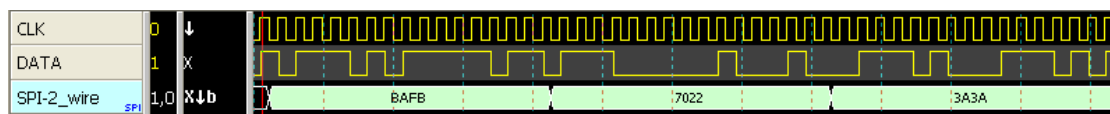


If the chip slave is not used and the interval between frames is not 0. You can set the interval as 6us, any data bit higher than 6us will be seen as Idle.





If the chip slave is not used and the interval between frames is 0. You can see the data continuous as the dialog below.



SPI Settings

Setting

Type
2 Wire-SPI(Unused Chip Slave)

☐ Use External clock

Clock Channel(SCK) A1

Bit Order MSB First

Word Size 8 bit (4~40)

Data valid from SCK 0 S/R Clk

Report

☒ Show Idle state in report window

☐ Reduce report

Show data in report (Column) 8

2 Wire-SPI(Unused Chip Slave)

Data Channel (SDA) A0

Data Edge Rising

☐ SDI(Write)-Latency-SDO(Read)

Write Length 8 Latency 2

Read Length 8 (Bits)

Frame guard time 300 ns

SCK

SDA

Color

SDI/SDA/Write Channel

SDO/Read Channel

Range

Decode Range

From Buffer Head To Buffer Tail

Default OK Cancel

We also offer bi-direction mode as the dialog below.

☒ SDI(Write)-Latency-SDO(Read)

Write Length 8 Latency 2

Read Length 8 (Bits)

Frame guard time 300 ns

SCK

SDA

Write

Read

Check the SDI(Write)-Latency-SDO(Read) to set the bit numbers for the 3 columns;

Write and Read (1~65535), Latency (0~65535).

Bit Order: MSB first or LSB first.

Word size: Default is 8 bits, minimum is 4 and maximum is 32.

Report: Show Idle state in report window, You can disable this default for not to display the idle state on the Report Window.

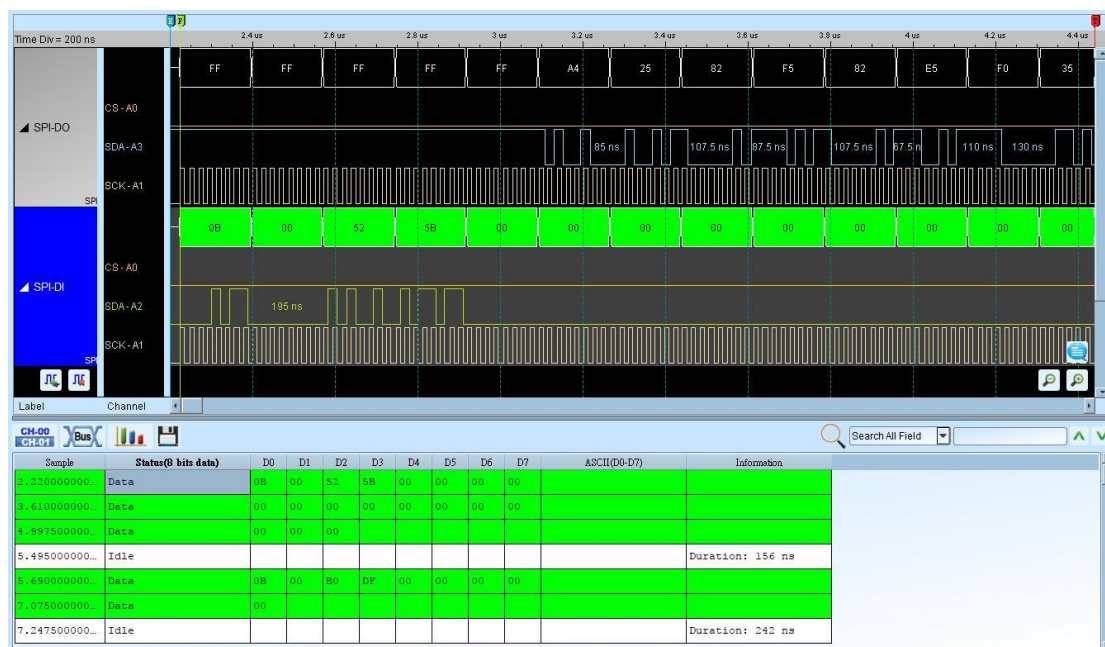
Show data in report: Display the ASCII code with default 16 columns on the Report Window.

Data Valid from SCK: In some SPI devices, the data is not valid right after the data output or the clock edge. You can set the data valid after 0-3 units of the sampling rate in Data valid from SCK; if the unit is 1 and the sampling rate is 200MHz, the delay time is 5 ns.

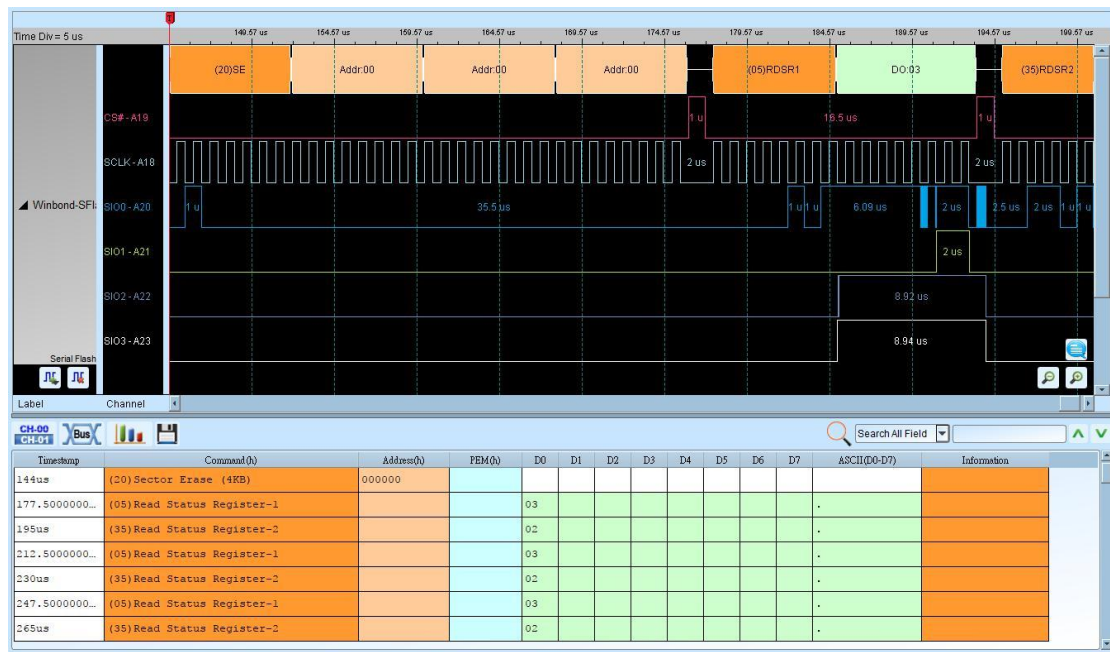
Result

Click **OK** to run the SPI decode and see the result on the Waveform Window below.

3-Wire SPI, Internal clock mode



3-Wire SPI, External clock mode



Serial Peripheral Interface NAND (SPI NAND)

SPI NAND Flash is a SPI/QPI interfaced NAND flash memory. The decoder translates the bus signal to command/address/data field to provide an easier way to exam the SPI NAND waveform.

Settings

SPI NAND Settings

Parameter Settings

CS# A0 SCK A1 Micron

SI/SO0 A2 SO/SO1 A3 MT29FXG01AAADD

WP/SO2 A4 HOLD#/SO3 A5

☐ Refer to #Hold status

Start up reading mode Continuous Read

Command deselect time 50ns

Clock LOW to output valid 15ns

Color

OpCode Address Data Out Dummy Data In

Range

Decode Range From To

Buffer Head Buffer Tail

Default OK Cancel

CS#: Chip select

SCLK: Clock

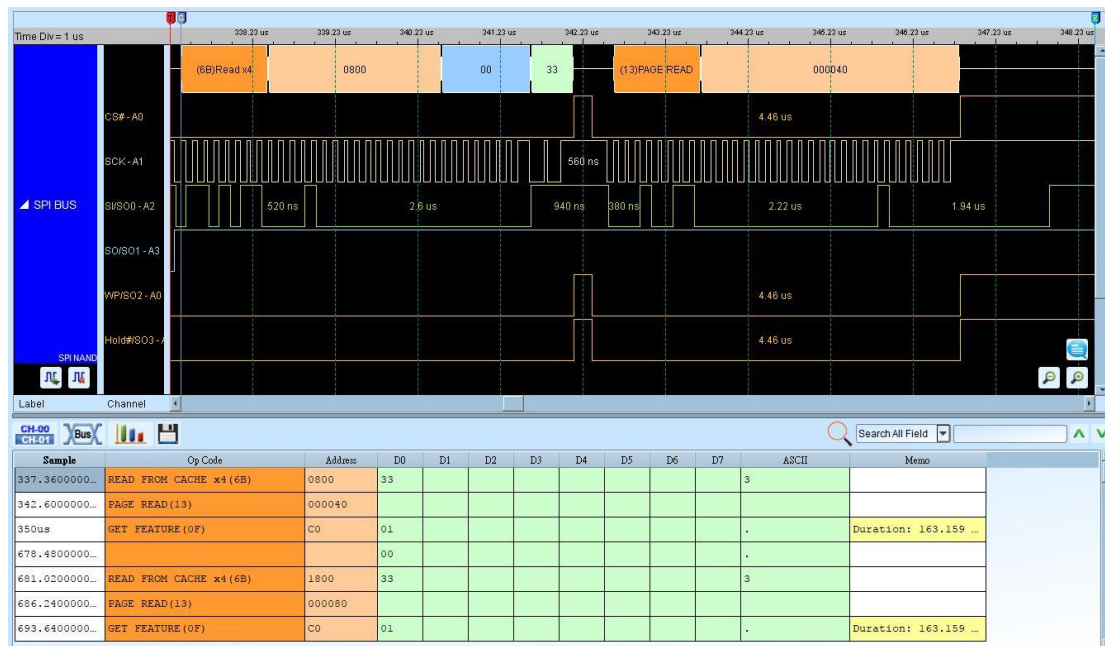
SIO0 – SIO3: Data

Start up reading mode: The initial setting of the reading mode for the decoder.

Command deselect time: The minimum required time for #CS deselecting. Clock

LOW to output valid: The data probe time after clock falling.

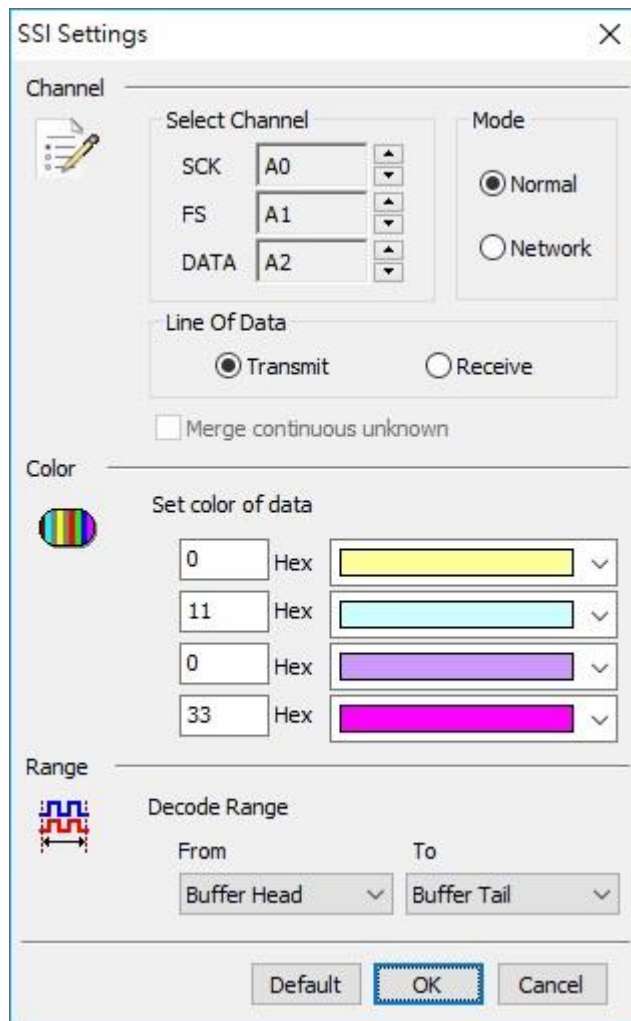
Result



SSI

The Synchronous Serial Interface (SSI) protocol has four kinds of signals: Serial Clock (SCK), Transmit Data, Receive Data and Transmit/Receive Frame Synchronous (FS). The SSI protocol supports either the Normal or Network mode that is independent of whether the transmitter and the receiver are synchronous or asynchronous.

Settings



The SSI Settings dialog box is divided into three main sections: Channel, Color, and Range. The Channel section includes a 'Select Channel' area with three rows: SCK (A0), FS (A1), and DATA (A2), each with up and down arrow buttons. To the right is a 'Mode' section with two radio buttons: 'Normal' (selected) and 'Network'. Below this is a 'Line Of Data' section with two radio buttons: 'Transmit' (selected) and 'Receive'. A checkbox 'Merge continuous unknown' is located below the 'Line Of Data' section. The Color section features a 'Set color of data' area with four rows, each containing a numeric value, the text 'Hex', and a color selection box. The values are 0, 11, 0, and 33, with corresponding colors of yellow, cyan, purple, and magenta. The Range section includes a 'Decode Range' area with two dropdown menus: 'From' (set to 'Buffer Head') and 'To' (set to 'Buffer Tail'). At the bottom are three buttons: 'Default', 'OK' (highlighted with a blue dashed border), and 'Cancel'.

Signal	Channel
SCK	A0
FS	A1
DATA	A2

Mode: ☒ Normal ☐ Network

Line Of Data: ☒ Transmit ☐ Receive

☐ Merge continuous unknown

Set color of data:

Value	Hex	Color
0	Hex	Yellow
11	Hex	Cyan
0	Hex	Purple
33	Hex	Magenta

Decode Range:

From	To
Buffer Head	Buffer Tail

Buttons: Default, OK, Cancel

Select Channel: Show the selected channels.

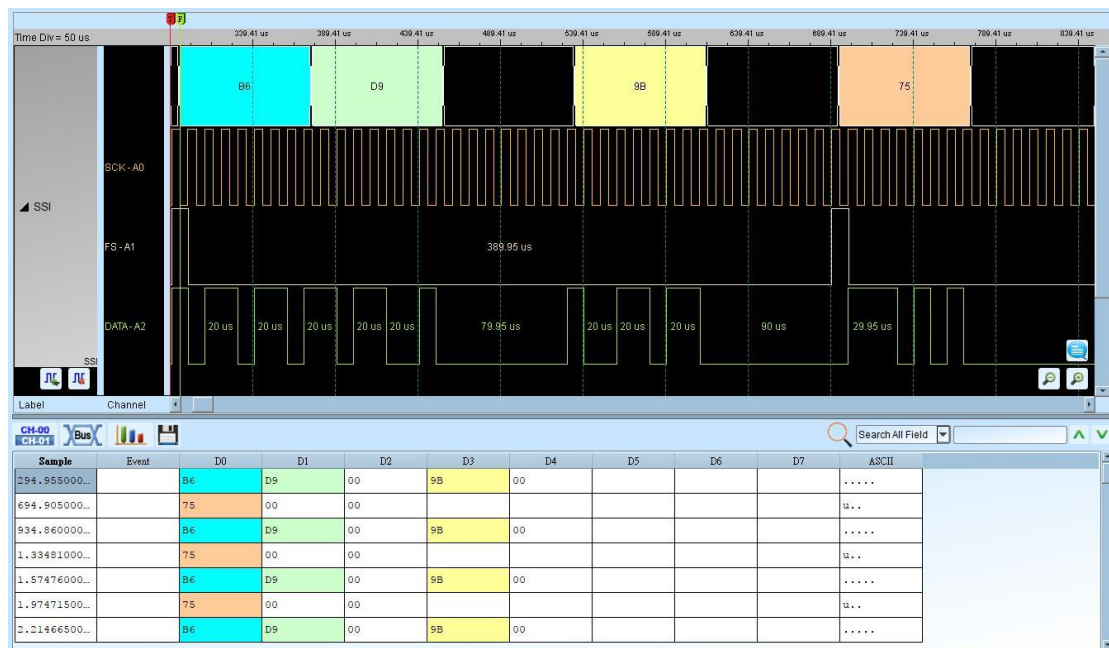
Mode: Normal or Network.

Line Of Data: Transmit or Receive.

Merge continuous unknown: Combine the unknown data only in Network mode.

Result

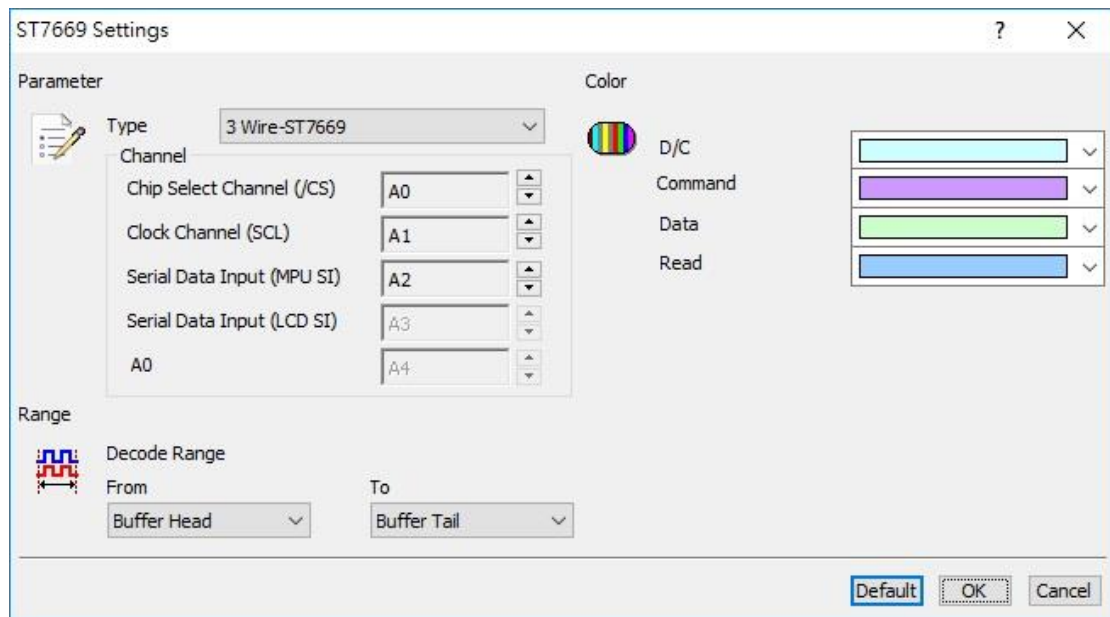
Click **OK** to run SSI decode and see the result on the Report Window below.



ST7669

ST76669 was developed by Sitronix to interface with the LCD module.

Settings

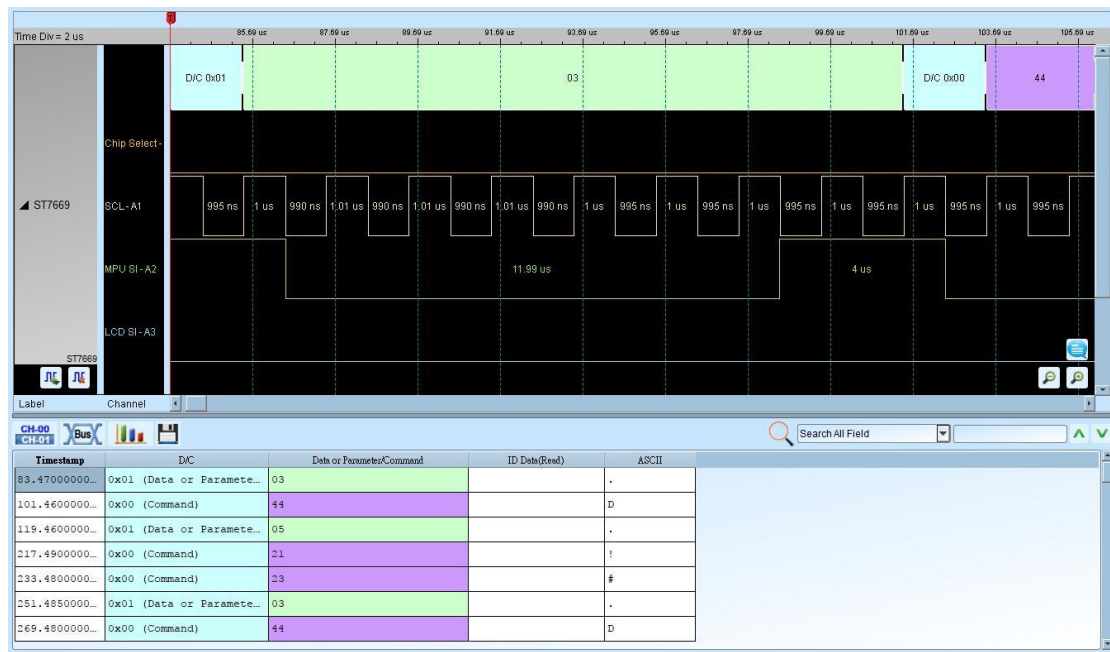


The ST7669 Settings dialog box is used to configure the interface with the LCD module. It includes a 'Parameter' section with a 'Type' dropdown set to '3 Wire-ST7669' and a 'Channel' section with five input fields: 'Chip Select Channel (/CS)' set to A0, 'Clock Channel (SCL)' set to A1, 'Serial Data Input (MPU SI)' set to A2, 'Serial Data Input (LCD SI)' set to A3, and 'A0' set to A4. Each field has up and down arrow buttons. To the right is a 'Color' section with a color bar icon and four color-coded dropdowns: 'D/C' (cyan), 'Command' (purple), 'Data' (green), and 'Read' (blue). At the bottom left is a 'Range' section with a waveform icon and a 'Decode Range' section containing 'From' and 'To' dropdowns, both set to 'Buffer Head' and 'Buffer Tail' respectively. At the bottom right are 'Default', 'OK', and 'Cancel' buttons.

Channel: Show the selected channels.

Result

Click **OK** to run the LCD1602 decode and see the result on the Waveform Window below.

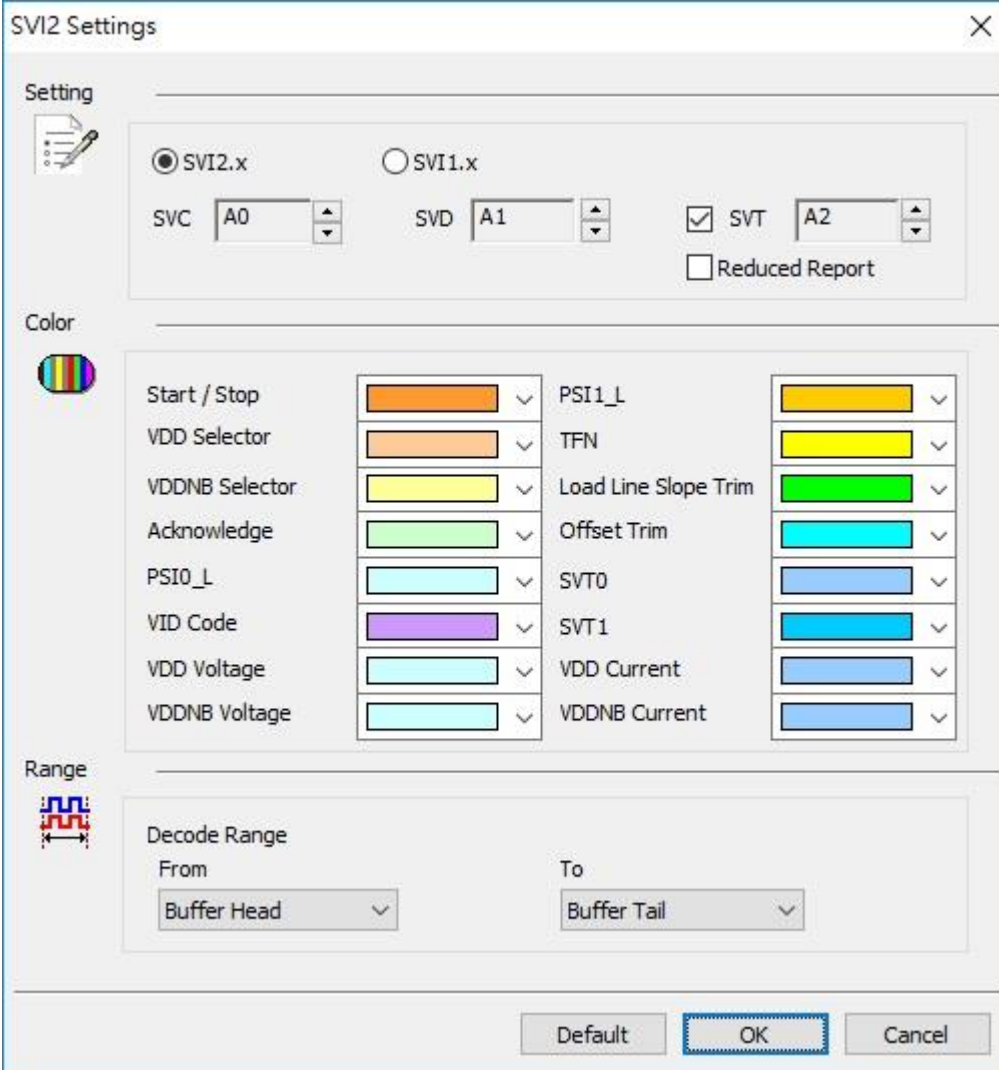


Serial VID Interface 2.0 (SVI2)

The SVI2 protocol is an interface for power management and developed by AMD.

The SVI2 working voltage is between 1V to 1.6V and its maximum frequency is at 20MHz with 3 bits : SVC/ SVD/ SVT.

Settings



The SVI2 Settings dialog box is divided into three main sections: Setting, Color, and Range.

Setting: This section contains radio buttons for **SVI2.x** (selected) and **SVI1.x**. Below these are three dropdown menus for **SVC** (set to A0), **SVD** (set to A1), and **SVT** (set to A2). There is also a checkbox for **Reduced Report** which is currently unchecked.

Color: This section features a color calibration icon and a grid of 14 color selection boxes, each with a dropdown arrow. The items are arranged in two columns:
Left column: Start / Stop, VDD Selector, VDDNB Selector, Acknowledge, PSIO_L, VID Code, VDD Voltage, VDDNB Voltage.
Right column: PSI1_L, TFN, Load Line Slope Trim, Offset Trim, SVT0, SVT1, VDD Current, VDDNB Current.

Range: This section includes a waveform icon and a **Decode Range** section with two dropdown menus: **From** (set to Buffer Head) and **To** (set to Buffer Tail).

At the bottom of the dialog are three buttons: **Default**, **OK** (highlighted with a blue border), and **Cancel**.

SVC: SVI2 clock.

SVD: SVI2 data.

SVT: SVI2 telemetry data line. Telemetry will not be decoded if the SVT is not

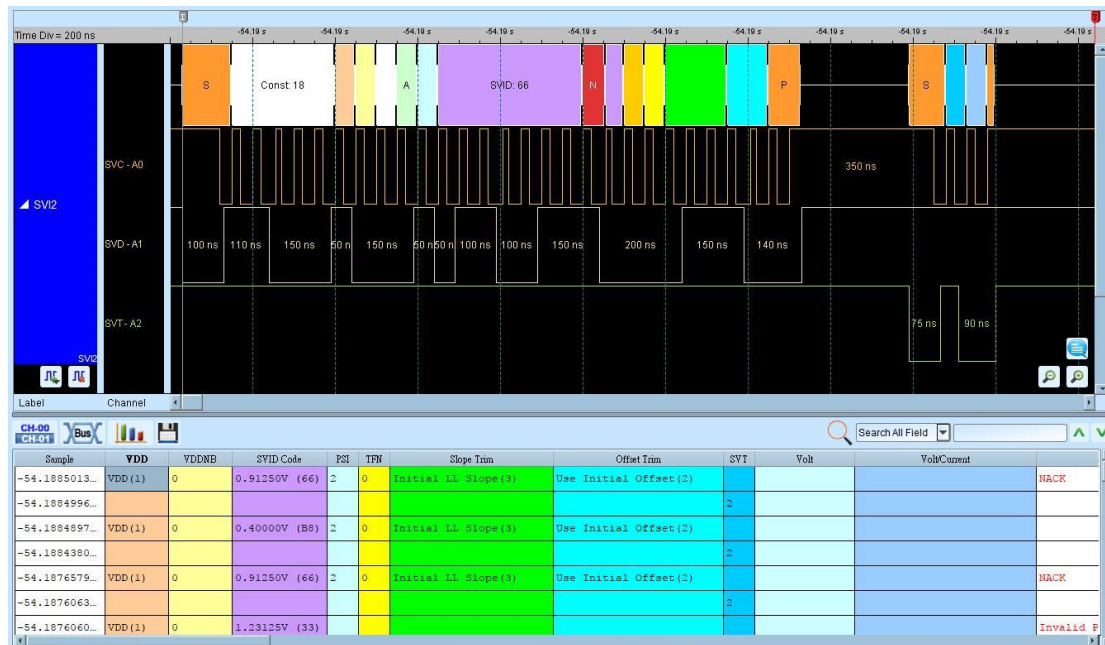
checked.

SVI2.x / SVI1.x: Select SVI2 / SVI protocol to decode.

Reduced Report: Only show SVD / VOTFC packet in the report window.

Result

Click **OK** to run the SVI2 decode and see the result on the Waveform Window below.



Serial VID (SVID)

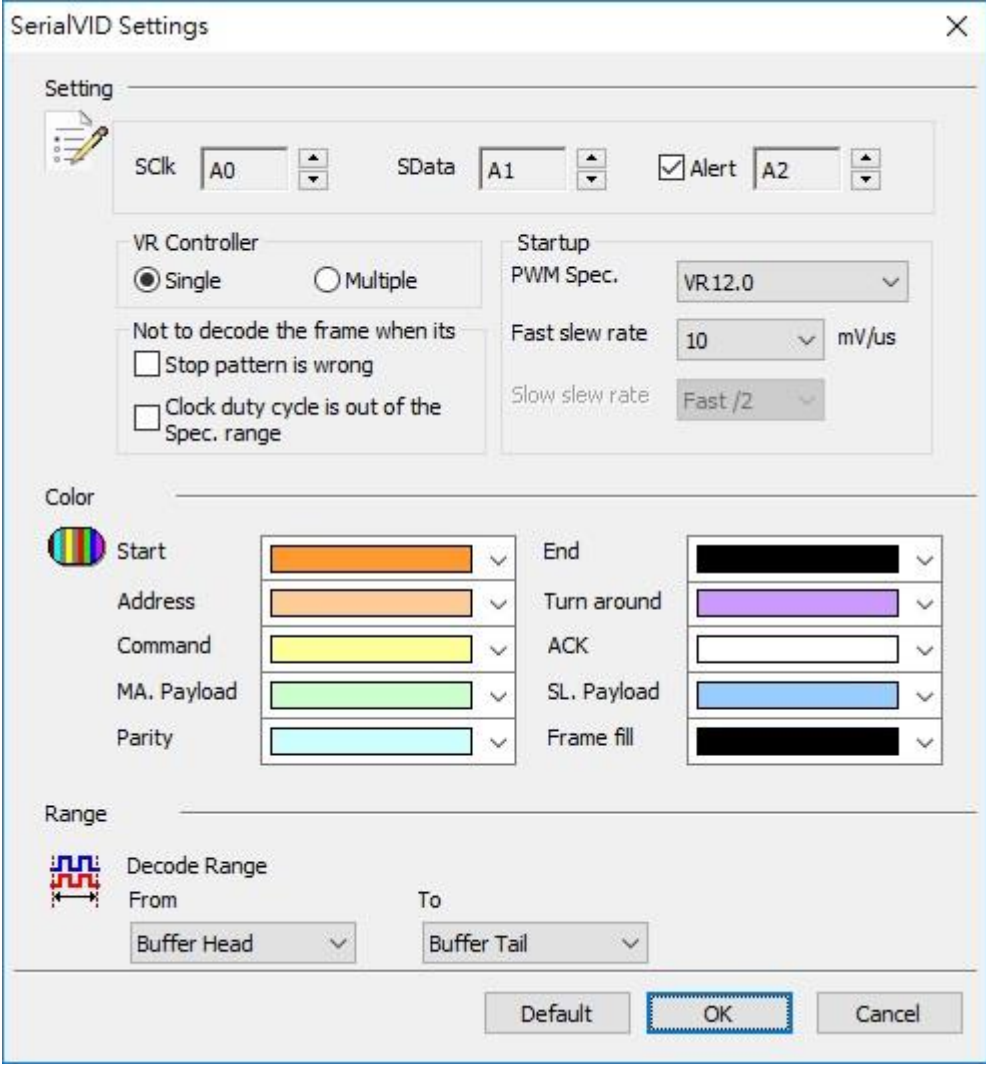
Serial VID (SVID) protocol is for power management and developed by Intel. SVID voltage is between 1.0V to 1.1V, maximum frequency at 26.25MHz and is 3 wires : SCLK/ SDATA/ ALERT.

Supported version:

IMVP7/VR12, VR12.1, VR12.5, VR12.6

IMVP8/VR13

Settings



The image shows the 'SerialVID Settings' dialog box. It is divided into three main sections: 'Setting', 'Color', and 'Range'. The 'Setting' section includes fields for SCLK (A0), SDATA (A1), and Alert (A2) pins, with a checked 'Alert' checkbox. It also has radio buttons for 'VR Controller' (Single selected, Multiple unselected) and checkboxes for 'Not to decode the frame when its Stop pattern is wrong' and 'Clock duty cycle is out of the Spec. range'. The 'Startup' section has a 'PWM Spec.' dropdown set to 'VR12.0', and 'Fast slew rate' (10 mV/us) and 'Slow slew rate' (Fast /2) dropdowns. The 'Color' section has a 'Start' color icon and two columns of color pickers for 'End', 'Turn around', 'ACK', 'SL. Payload', and 'Frame fill'. The 'Range' section has a 'Decode Range' icon and 'From' (Buffer Head) and 'To' (Buffer Tail) dropdowns. At the bottom are 'Default', 'OK', and 'Cancel' buttons.

Setting	Value
SCLK	A0
SDATA	A1
Alert	<input checked="" type="checkbox"/> A2
VR Controller	Single
Not to decode the frame when its Stop pattern is wrong	<input type="checkbox"/>
Clock duty cycle is out of the Spec. range	<input type="checkbox"/>
Startup PWM Spec.	VR12.0
Fast slew rate	10 mV/us
Slow slew rate	Fast /2

Color	Start	End	Turn around	ACK	SL. Payload	Frame fill
Start	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]
Address	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]
Command	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]
MA. Payload	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]
Parity	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]	[Color Picker]

Range	From	To
Decode Range	Buffer Head	Buffer Tail

Buttons: Default, OK, Cancel

SCK: SVID clock.

SData: SVID data.

Alert: Alert, optional reminder.

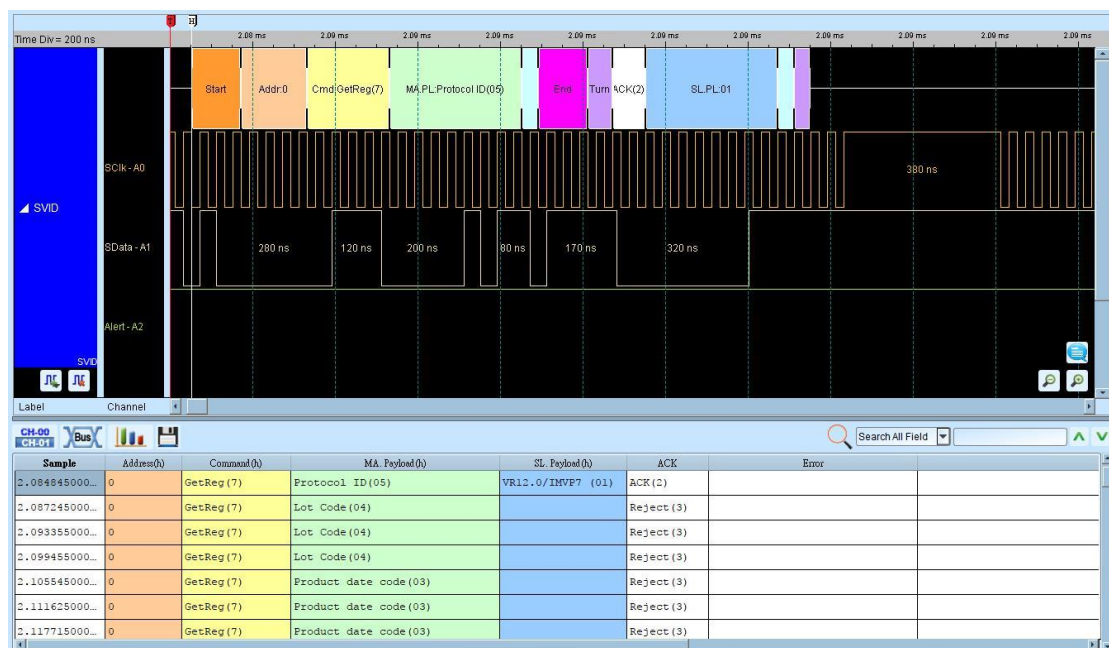
VR Controller: Set single or multiple controllers in current VR. Set different address.

Not to decode the frame when its stop pattern wrong or clock duty cycle is out of range.

Result

Click OK to run the SVID decode and see the result on the Waveform Window

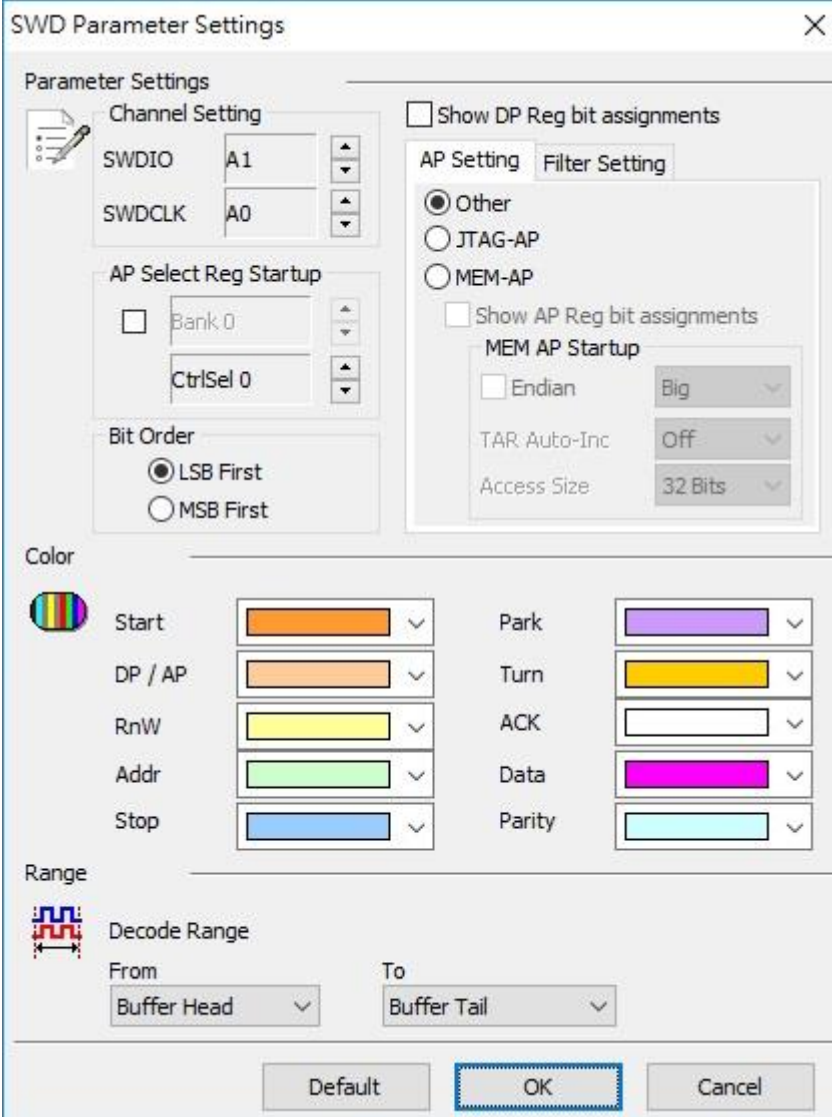
below.



Serial Wire Debug (SWD)

The SWD is a 2-pin electrical alternative JTAG interface that has the same JTAG protocol on top. It uses the existing GND connection. SWD uses an ARM CPU standard bi-directional wire protocol, defined in the ARM Debug Interface v5.

Settings



The image shows the 'SWD Parameter Settings' dialog box. It is divided into several sections: 'Parameter Settings' at the top, 'Color' in the middle, and 'Range' at the bottom. The 'Parameter Settings' section includes 'Channel Setting' with 'SWDIO' set to 'A1' and 'SWDCLK' set to 'A0'; 'AP Select Reg Startup' with 'Bank 0' and 'CtrlSel 0' selected; 'Bit Order' with 'LSB First' selected; and 'AP Setting' with 'Other' selected. The 'Color' section has a 'Color' icon and a table of color settings for Start, DP / AP, RnW, Addr, Stop, Park, Turn, ACK, Data, and Parity. The 'Range' section has a 'Decode Range' icon and 'From' and 'To' dropdowns set to 'Buffer Head' and 'Buffer Tail' respectively. At the bottom are 'Default', 'OK', and 'Cancel' buttons.

Color	Start	DP / AP	RnW	Addr	Stop	Park	Turn	ACK	Data	Parity
	Orange	Orange	Yellow	Green	Blue	Purple	Yellow	White	Magenta	Cyan

SWDIO: I/O data.

SWDCLK: Clock.

AP Select Reg Startup: When the AP Select Reg Startup is not assigned, only the

address information will be shown. You may input the Bank and Ctrl/Select initial values manually.

☐

Bank = 0

CtrlSel = 0

Time	Select	RnW	Address (h)	ACK	Data
-0.0003 ms	AP	Write	0	OK	23 00 00 52

☒

Bank = 0

CtrlSel = 0

Time	Select	RnW	Address (h)	ACK	Data
-0.0003 ms	AP	Write	Bank 0 Register 0 (0)	OK	23 00 00 52

Bit Order: LSB or MSB.

Show DP Reg bit assignments: Show the DP register information.

Select	RnW	Address (h)	ACK	Data
DP	Write	SELECT Register (8)	OK	00 00 00 00
				APSEL [31:24] 00
				APBANKSEL [7:4] 0
				CTRLSEL [0] 0

AP Setting:

JTAG-AP: Show the JTAG AP decode.

MEM-AP: Show the MEM AP decode.

Other: Show Bank X Register X.

<input checked="" type="radio"/> Other	Time	Select	RnW	Address (h)	ACK	Data
<input type="radio"/> JTAG-AP	-0.0003 ms	AP	Write	Bank 0 Register 0 (0)	OK	23 00 00 52
<input type="radio"/> MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	Bank 0 Register 1 (4)	OK	00 00 02 68
<input type="radio"/> Other	Time	Select	RnW	Address (h)	ACK	Data
<input checked="" type="radio"/> JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
<input type="radio"/> MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	PSEL Register (4)	OK	00 00 02 68
<input type="radio"/> Other	Time	Select	RnW	Address (h)	ACK	Data
<input type="radio"/> JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
<input checked="" type="radio"/> MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	TAR Register (4)	OK	00 00 02 68

Show AP Reg bit assignments: Display the AP register information if JTAG-AP or MEM-AP checked.

MEM-AP	Select	RnW	Address (h)	ACK	Data
<input checked="" type="checkbox"/> Show AP Reg bit assignments	AP	Read	BASE Register (8)	OK	00 00 00 00
					BASEADDR [31:12] E00FF
					Format [1] 1
					Entry present [0] 1

MEM AP Startup: Assign the initial MEM-AP value.

MEM-AP	AP	Read	DRW Register (C)	OK	00 00 00 0D	TAR Address = E000EFF0
<input checked="" type="checkbox"/> Show AP Reg bit assignments					Big-Endian	
					000D Access to E000EFF0	
					0000 Access to E000EFF2	
MEM AP Startup	AP	Read	DRW Register (C)	OK	00 00 00 E0	TAR Address = E000EFF2
<input checked="" type="checkbox"/> Endian Big					Big-Endian	
TAR Auto-Inc Single					00E0 Access to E000EFF2	
Access Size 16 Bits					0000 Access to E000EFF4	

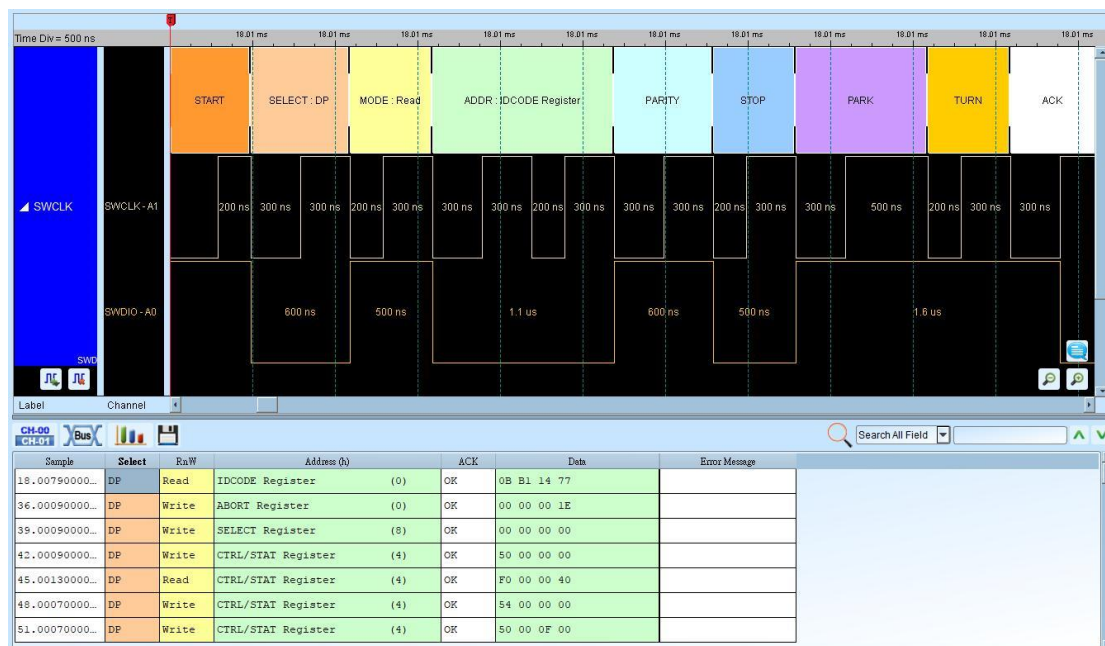
Filter Setting: Filter the unwanted Registers.

AP Setting Filter Setting

Register Display List

- ☒ DP - ABORT Register
- ☒ DP - IDCODE Register
- ☒ DP - CTRL/STAT Register
- ☒ DP - WCR Register
- ☒ DP - SELECT Register
- ☒ DP - RESEND Register
- ☒ DP - ROUTESEL Register
- ☒ DP - RDR1 IFF Register

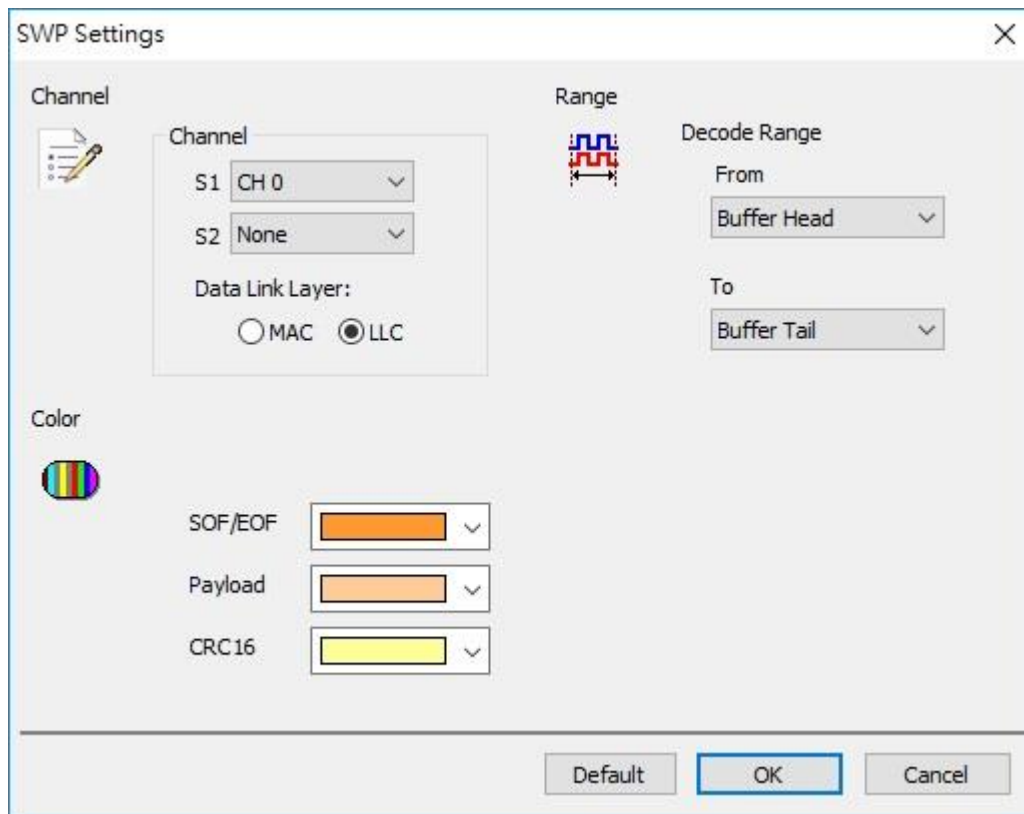
Result



SWP

The Single Wire Protocol (SWP) is a single-wire connection between the SIM card and a NFC chip in a cell phone.

Settings



S1: I/O data.

S2: I/O data in current domain and it need convert to voltage domain.

Data Link Layer: Supported MAC and LLC layers

Result



Universal Asynchronous Receiver/Transmitter (UART)

The UART (RS-232 or RS-485) protocol has two message types: Transmitter (TX) and Receiver (RX); you can measure the UART protocol in one signal or two signals.

RS-485 need convert to logic signal, because LA can not capture differential signal.

Settings

UART Settings

Parameter Settings

Channel

Tx A0

Rx A1

Polarity Idle high

☐ Auto Detect

Baud Rate 9600

Data Bits 8

Parity None

Stop Bits 1

☐ MSB first ☒ Show scale in the waveform

☐ Show Idle state in report window

Line Wrap Data

Users can assign Line Wrap Data as header of data. Default setting is 0A. (Hexadecimal)

☐ Line Wrap Data

1st Pattern 0A Color

2nd Pattern 0A

Range

Decode Range

From Buffer Head To Buffer Tail

Default OK Cancel

Data: Show the selected channel (CH0).

Rx: Show Rx data in report window.

Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Protocol: (Parity - Data Bits - Stop Bits)

Parity: N (None), O (Odd), or E (Even).

Data Bits: 5 to 10 bits.

Stop Bits: 1 to 2 bits.

MSB first: The default is LSB first; click it to change to MSB first.

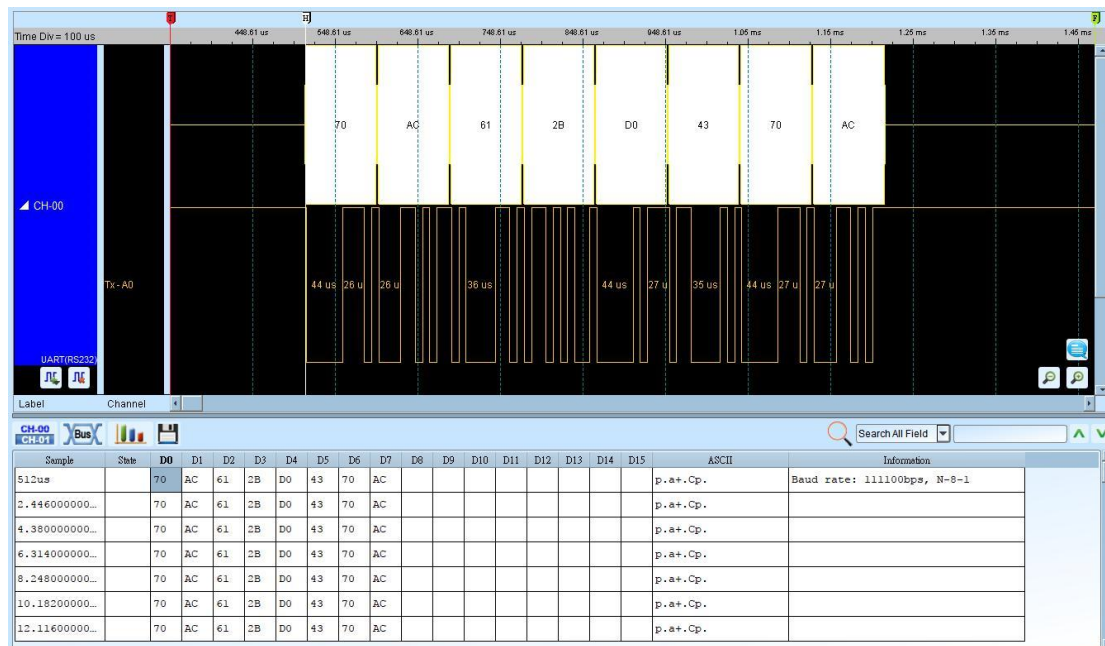
Report Unknown and Idle: Display the unknown and idle data in the Report Window.

Show scale in the waveform: Display the waveforms with scales.

Line Wrap Data: Use 1-2 value (hex) as header of data.

Result

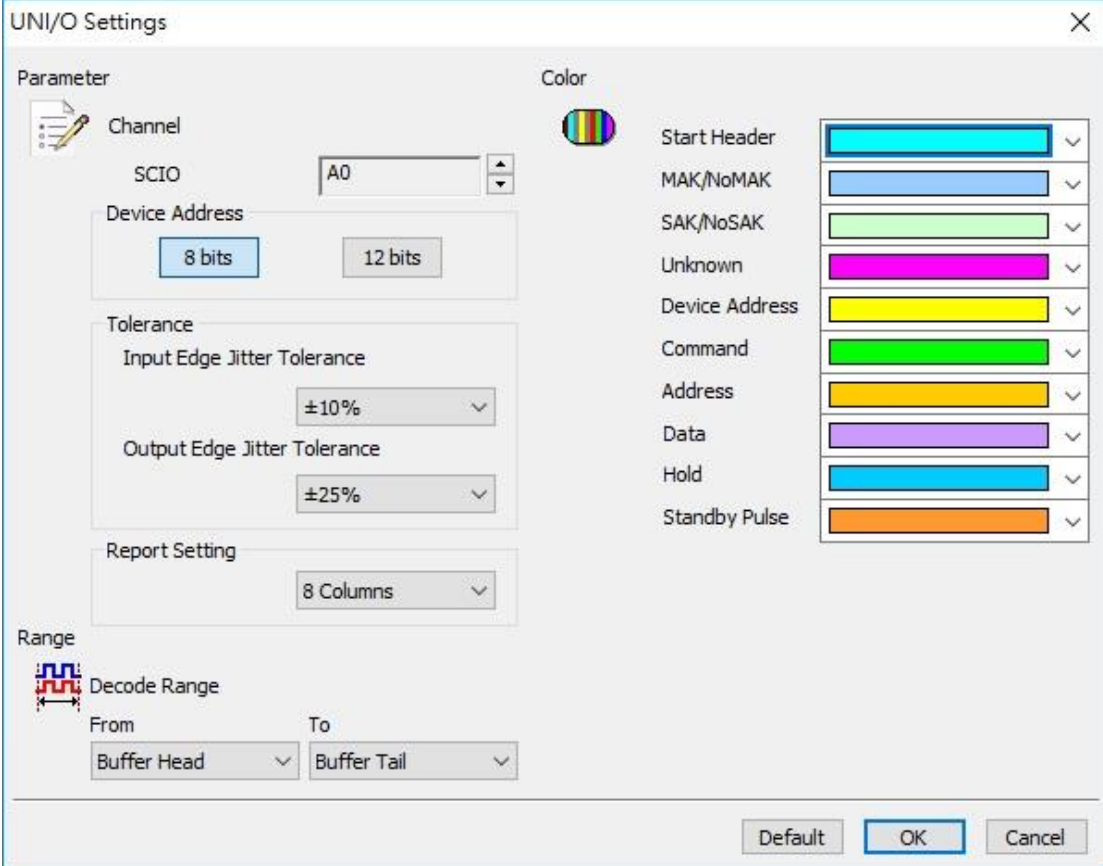
Click **OK** to run UART Decode and see result on the Waveform Window below.



UNI/O

The UNI/O interface was developed by Microchip. The data transfer rate is 10Kbps to 100Kbps.

Settings



The image shows the 'UNI/O Settings' dialog box. It is divided into several sections: 'Parameter' on the left, 'Color' on the right, and 'Range' at the bottom. The 'Parameter' section includes a 'Channel' dropdown set to 'SCIO', a 'Device Address' field with 'A0' and a spin button, two buttons for '8 bits' and '12 bits', 'Tolerance' settings for 'Input Edge Jitter Tolerance' (±10%) and 'Output Edge Jitter Tolerance' (±25%), and a 'Report Setting' dropdown set to '8 Columns'. The 'Color' section has a 'Color' icon and a list of items with corresponding color swatches: 'Start Header' (cyan), 'MAK/NoMAK' (blue), 'SAK/NoSAK' (green), 'Unknown' (magenta), 'Device Address' (yellow), 'Command' (bright green), 'Address' (orange), 'Data' (purple), 'Hold' (light blue), and 'Standby Pulse' (dark orange). The 'Range' section has a 'Decode Range' icon and two dropdowns for 'From' (set to 'Buffer Head') and 'To' (set to 'Buffer Tail'). At the bottom are 'Default', 'OK', and 'Cancel' buttons.

Parameter	Value
Channel	SCIO
Device Address	A0
Device Address Bits	8 bits
Input Edge Jitter Tolerance	±10%
Output Edge Jitter Tolerance	±25%
Report Setting	8 Columns

Color	Color
Start Header	Cyan
MAK/NoMAK	Blue
SAK/NoSAK	Green
Unknown	Magenta
Device Address	Yellow
Command	Bright Green
Address	Orange
Data	Purple
Hold	Light Blue
Standby Pulse	Dark Orange

Range	From	To
Decode Range	Buffer Head	Buffer Tail

Channel: Show the selected channels (SCIO CH0).

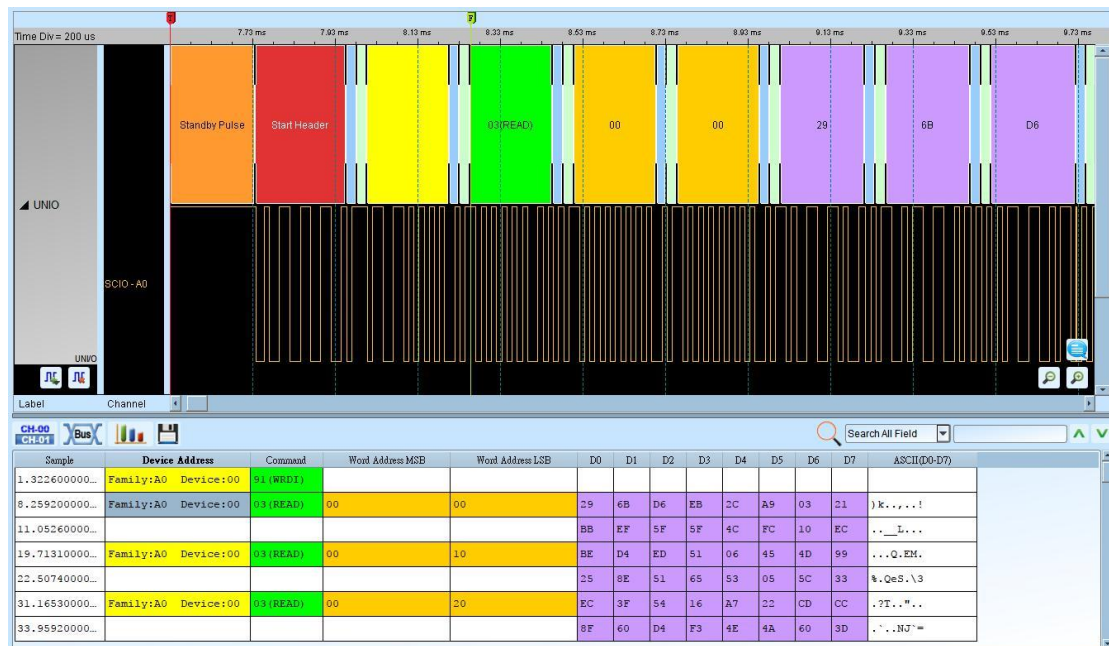
Device Address: Set data bits for the device address.

Tolerance: Set the Input / Output Edge Jitter Tolerance, ±10% / ±25% default.

Report Setting: To show the data by 8 or 16 columns in the Report Window.

Result

Click **OK** to run the UNI/O decode and see the result on the Waveform Window below.



USB1.1

The USB 1.0 specification was introduced in 1994. USB signals are transmitted on a twisted pair data cable with 90 Ohm $\pm 15\%$ impedance, labeled D+ and D-.

Settings

USB1.1 Settings

Parameter

Channel

D+ A0

D- A1

USB 1.1 Setting

☒ Auto Detect ☐ Low speed ☐ Full speed

☐ Decode USB standard request & descriptor

Report Setting

Mark PID SOF

Show Data 8 Column

PID Filter

☐ SOF ☐ DATA1

☐ SETUP ☐ ACK

☐ IN ☐ NACK

☐ OUT ☐ STALL

☐ DATA0 ☐ PRE

☐ Show scale in the waveform

Range

Decode Range

From Buffer Head To Buffer Tail

Color

Sync

Packet ID

Frame No. / Address / Endpoint / Data

CRC5/CRC16

EOP

Host To Device / Device To Host

Type

Recipient

bRequest

wValue

wIndex

wLength

Descriptor

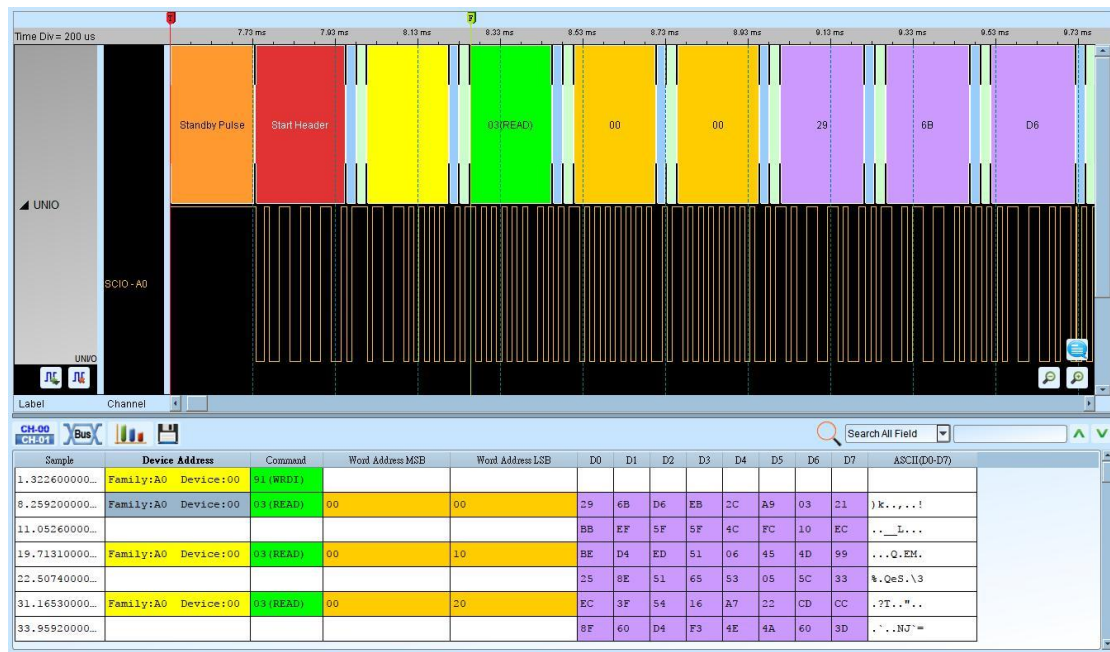
Default Ok Cancel

Channel: Show the selected channels (D+ CH0 and D- CH1).

USB1.1 Setting: Select USB state (low speed or full speed) and decode the USB standard request and descriptor.

Result

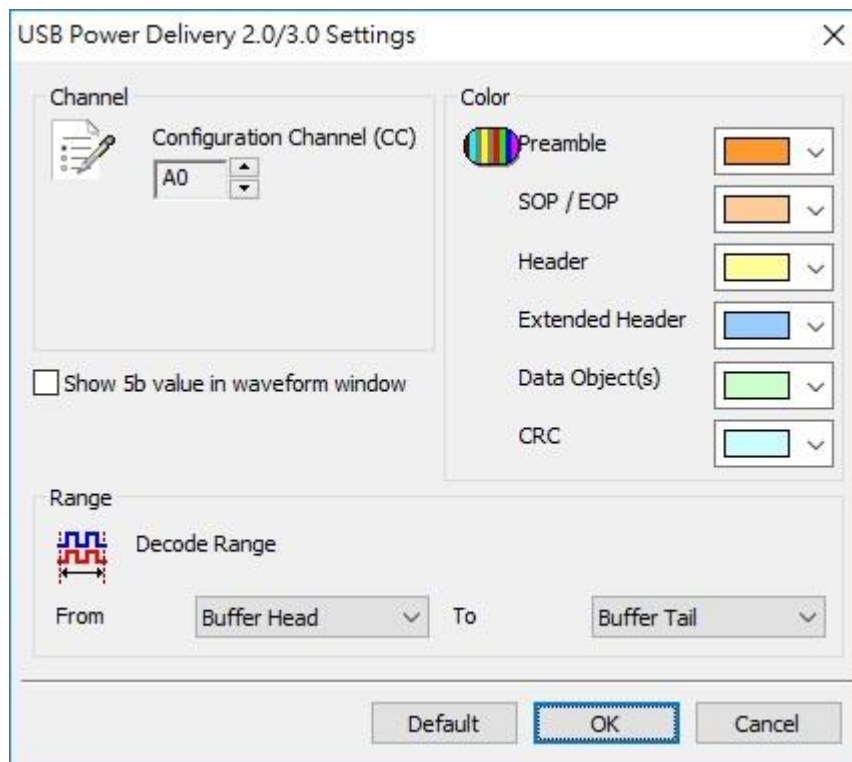
Click **OK** to run the USB1.1 decode and see the result on the Waveform Window.



USB PD 2.0/3.0

USB PD (Power Delivery) 2.0 is the protocol based on BMC (Biphase Mark Coding) and can be applied to Laptops / Tablets / Mobile phones / Power banks or other devices with USB Type-C for power supplying or charging. The maximum power offered by USB Type-C can be 100W, and the users can charge the device by supporting USB Type-C connector.

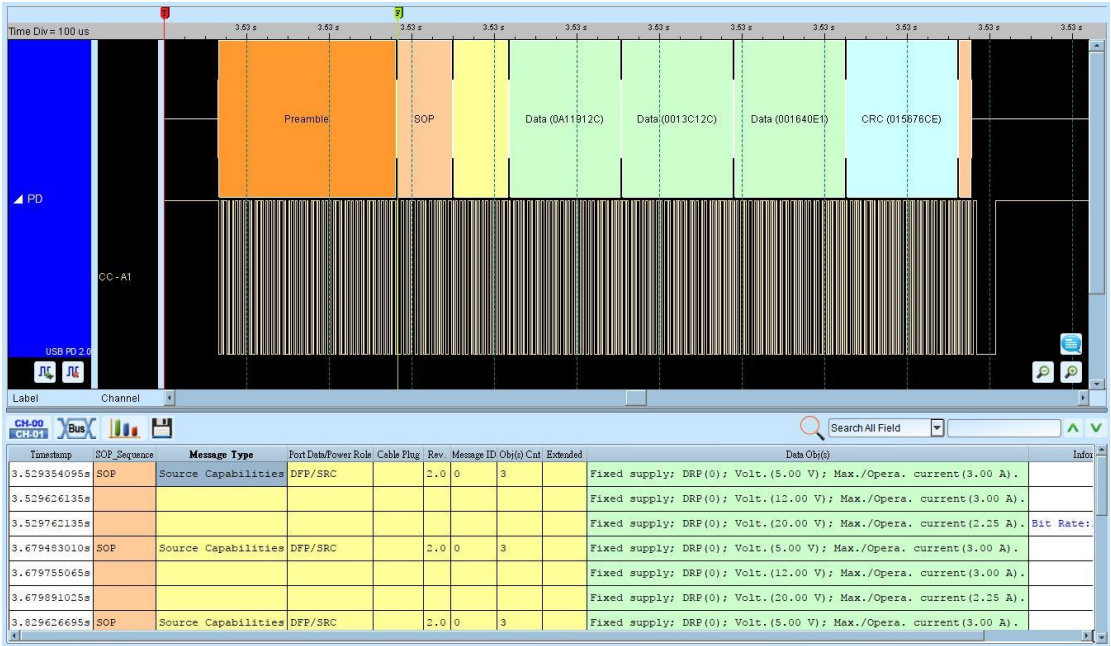
Settings



Channel: Set Configuration Channel (CC).

Show 5b value in waveform window: Show 4b or 5b value in the waveform.

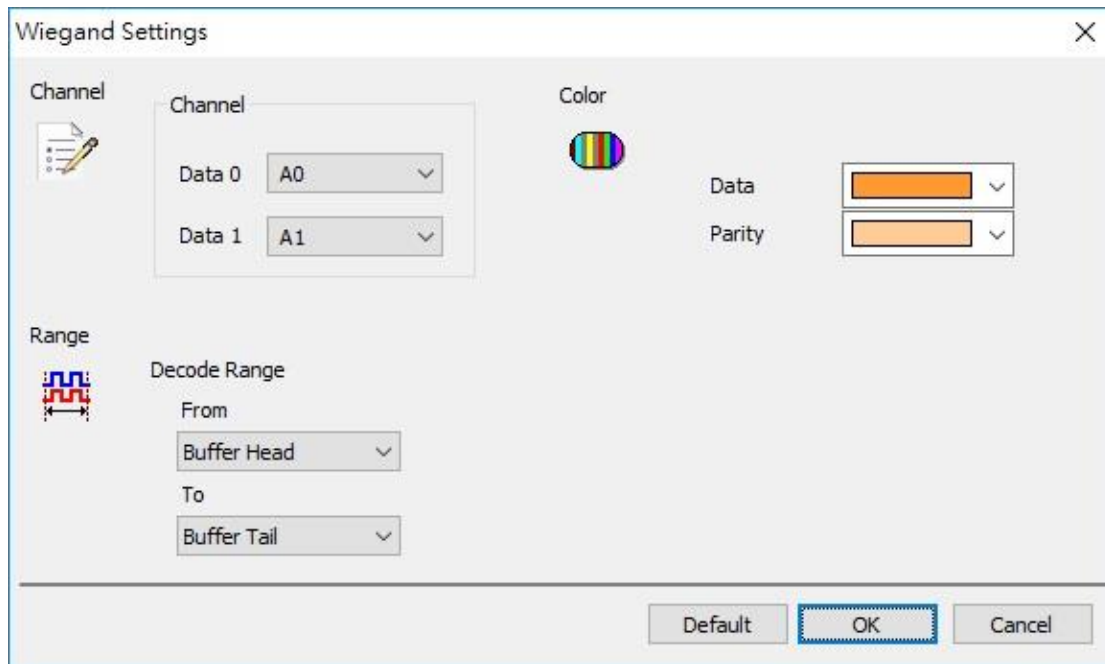
Result



Wiegand

It is commonly used to connect a card swipe mechanism to the rest of an electronic entry system..

Settings



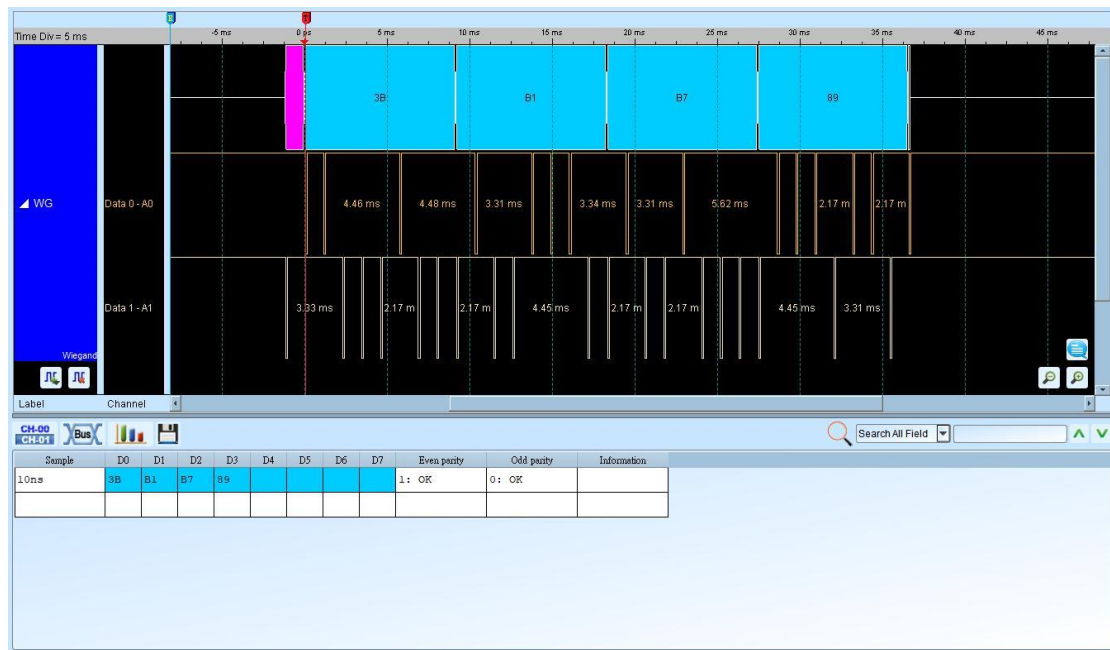
The Wiegand Settings dialog box is used to configure the decoding of Wiegand signals. It includes sections for Channel selection, Color selection, and Range selection. The Channel section has dropdowns for Data 0 (A0) and Data 1 (A1). The Color section has a color wheel icon and dropdowns for Data and Parity. The Range section has a waveform icon and dropdowns for Decode Range (From: Buffer Head, To: Buffer Tail). At the bottom are buttons for Default, OK, and Cancel.

Section	Parameter	Value
Channel	Data 0	A0
	Data 1	A1
Color	Data	[Orange]
	Parity	[Light Orange]
Range	From	Buffer Head
	To	Buffer Tail

Channel: Show the selected channels (Data 0 and Data 1).

Result

Click **OK** to run the wiegand decode and see the result on the Waveform Window.



Chapter 2 Bus Trigger

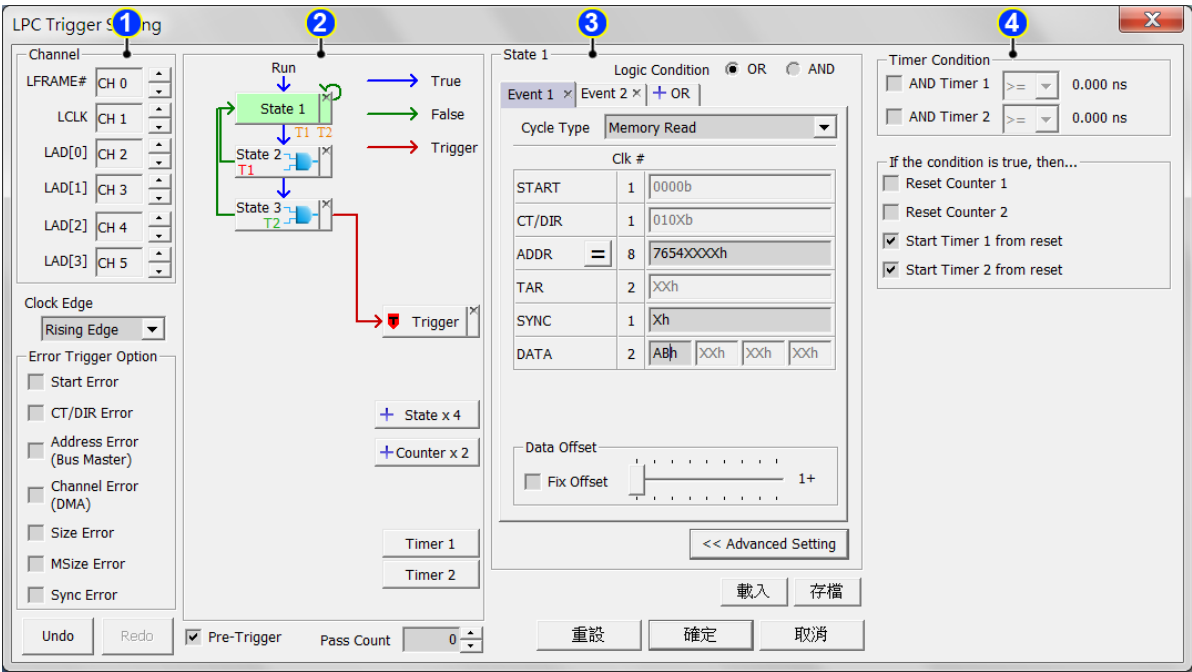
Bus Trigger

The bus trigger are only available for the POKEANA UPLA Series.

Bus Trigger	UPLA-2G34-8GP3	UPLA-2G34-1GP2	UPLA-1G17-16M P0	UPLA-1G34-1GP1
CAN	⊙	⊙		
eSPI	⊙			
I2C	⊙	⊙	⊙	⊙
I2S	⊙	⊙		
LIN	⊙	⊙		
LPC	⊙	⊙		
MIPI SPMI	⊙			
NAND Flash	⊙			
SD/eMMC	⊙			
Serial Flash	⊙			
SMBus/PMBus	⊙	⊙		
SPI	⊙	⊙		⊙
SVI2	⊙	⊙		
SVID	⊙	⊙		
UART	⊙	⊙		⊙
USB 1.1	⊙	⊙		

Clause trigger

The Clause trigger settings dialog box is as below.

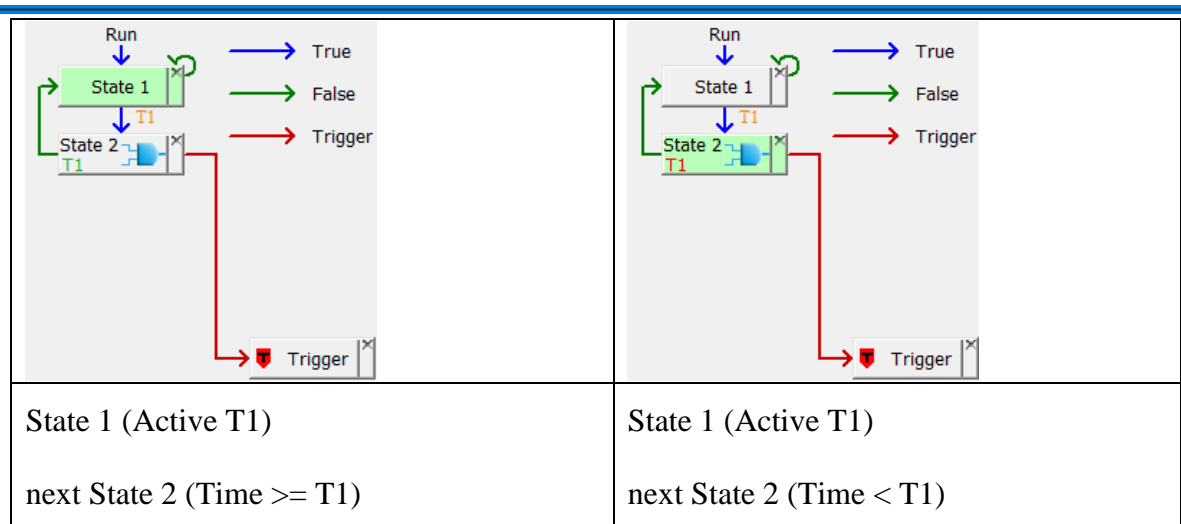


1. Channel and bus trigger settings:

Please refer to the descriptions in each bus trigger settings section.

2. Flow chart

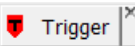
State 1 next State 2	State 1 then State 2	State 1 next State 2 then State 3 next State 4



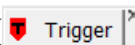
A state button represents a trigger state. The true state condition will only lead the branch to the next state, on the other hand, the false state condition could lead the branch to any state as below:


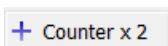
Click state 1 and state 2, then state 1 will branch to state 2 while state 1 is false.

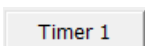
Double click any state, the state will branch to itself if it is false.

Click the state button and trigger button (): triggere when the state conditions is satisfied.

Delete any state by clicking the cross sign on the state.

Clear the links to the trigger button by clicking on the trigger button ()

Click  and  to add a new state.

 : The timer ranges from 5 ns to 8 days.

3. State settings

State 1

Logic Condition ☒ OR ☐ AND

Event 1 × Event 2 × + OR

Cycle Type Memory Read

	Clk #	
START	1	0000b
CT/DIR	1	010Xb
ADDR	8	7654XXXXh
TAR	2	XXh
SYNC	1	Xh
DATA	2	ABh XXh XXh XXh

Data Offset

☐ Fix Offset

The trigger conditions of the state:

1. The current state index
2. Logic condition between every event in the state.
3. Switch between the tab windows to edit the trigger events . Click **+ OR** / **+AND** to add new events (up to 8 events).
4. The bus trigger settings.

The relations between events and the trigger condition:

	AND	OR
Event settings	<div> <div>State 1</div> <div>X5h</div> <div>AND</div> <div>1Xh</div> </div> → <div> <div>State 2</div> <div>20h</div> </div>	<div> <div>State 1</div> <div>05h</div> <div>OR</div> <div>10h</div> </div> → <div> <div>State 2</div> <div>20h</div> </div>
Trigger condition	<div>15h</div> → <div>20h</div>	<div>05h</div> → <div>20h</div> OR <div>10h</div> → <div>20h</div>

4. Timer and Counter settings

Press Advanced Setting >> button to edit the timer/counter reset settings of the state.

Timer Condition

☒ AND Timer 1 < 5.000 ns

☒ AND Timer 2 >= 5.000 ns

If the condition is true, then...

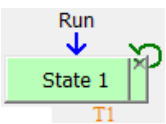
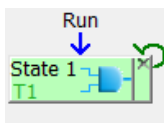
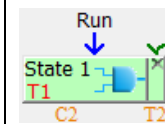
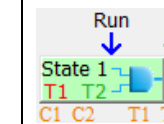
☒ Reset Counter 1

☒ Reset Counter 2

☒ Start Timer 1 from reset

☒ Start Timer 2 from reset

The following table describes the state button icons:

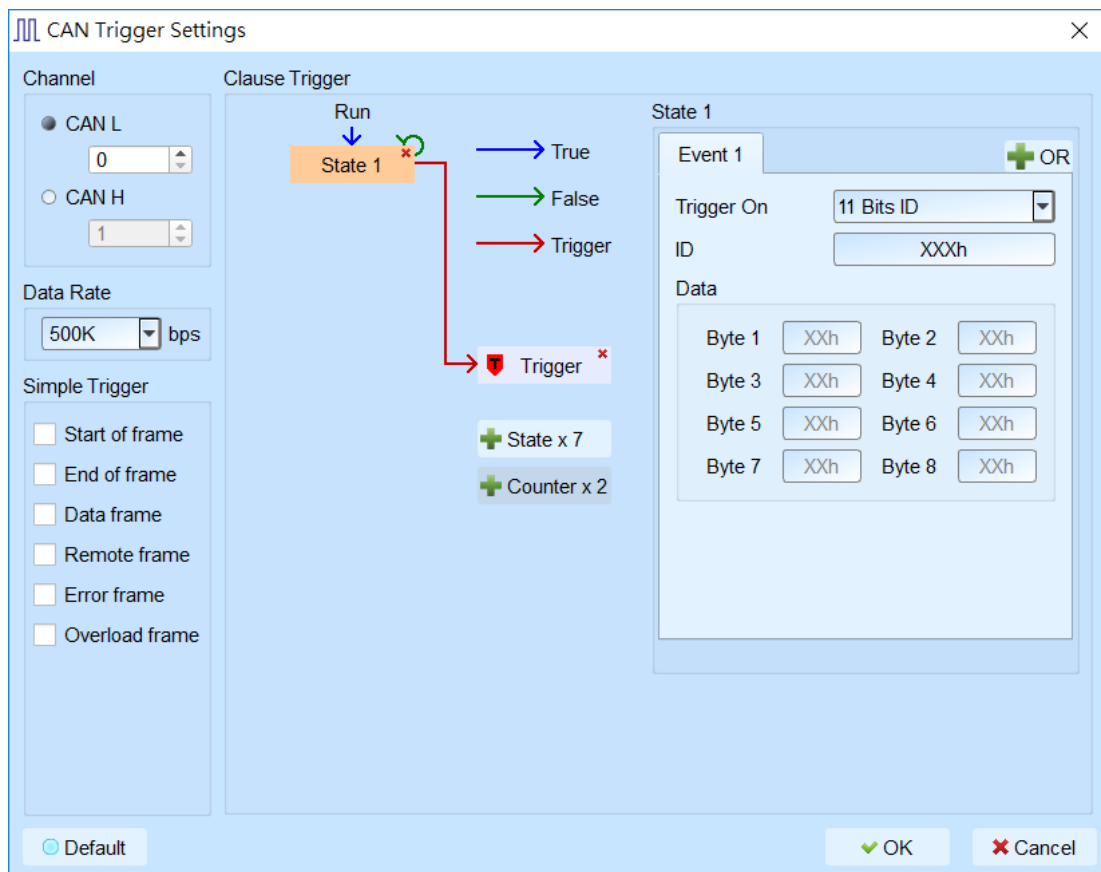
				
Conditions	State 1	State 1 And timer > T1	State 1 And timer < T1	State 1 And T2 < timer < T1
satisfied condition	Start T1	X	Start T2 Reset C2	Start T1 and T2 Reset C1 and C2

CAN Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

CAN Trigger Settings

Click CAN Trigger in the toolbar and will show the dialog as the following °



1. **Channel:** Select CAN_H or CAN_L as the trigger channel.
2. **Data Rate:** CAN data rate. Users could type the data rate if no data rate is available.
3. **Simple Trigger:** Specific trigger function of CAN.
4. **Clause Trigger:** Please reference Clause Trigger chapter.

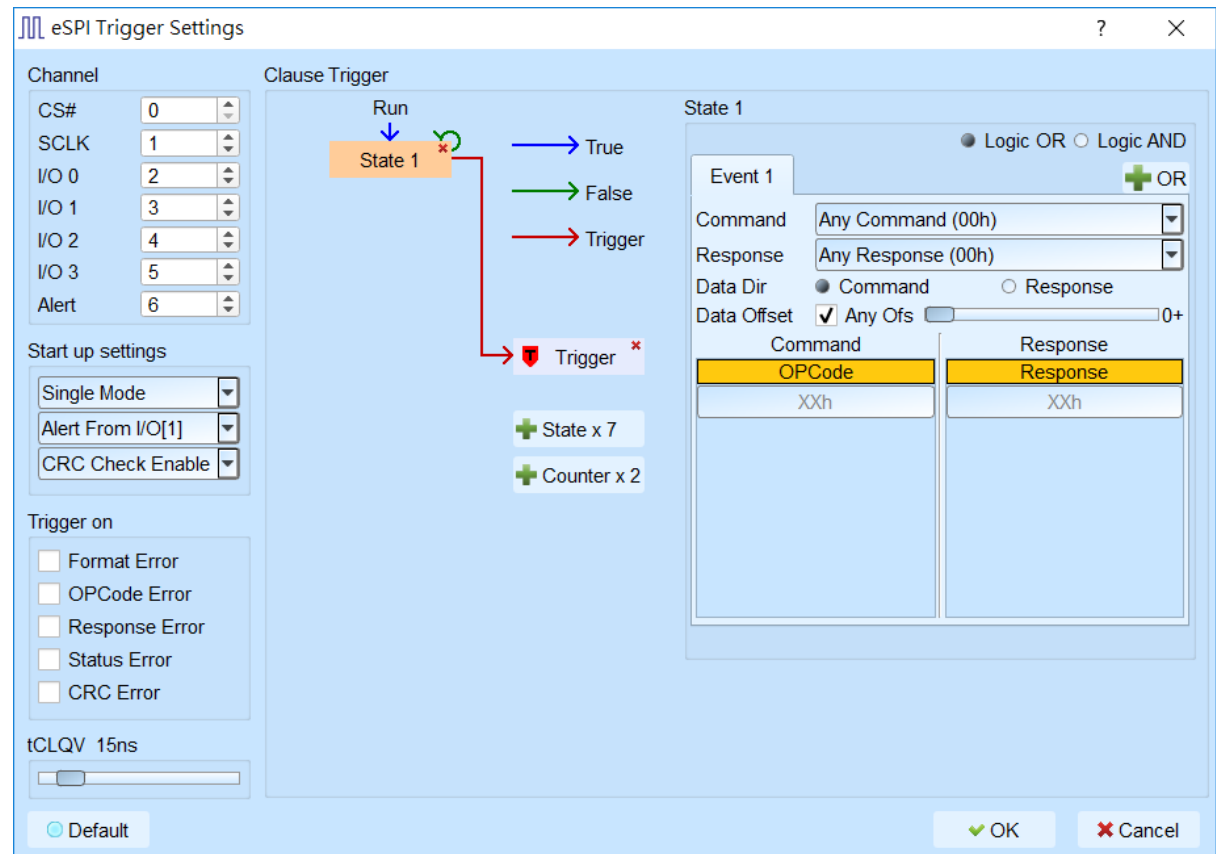
State: Show the details of trigger condition in every state as left side; typing the trigger values in the ID or Data fields, default value is XX means “don’t care”.

eSPI Trigger

Supported Models : UPLA-2G34-8GP3

eSPI Trigger Settings

Click eSPI Trigger in the toolbar and will show the dialog as the following.



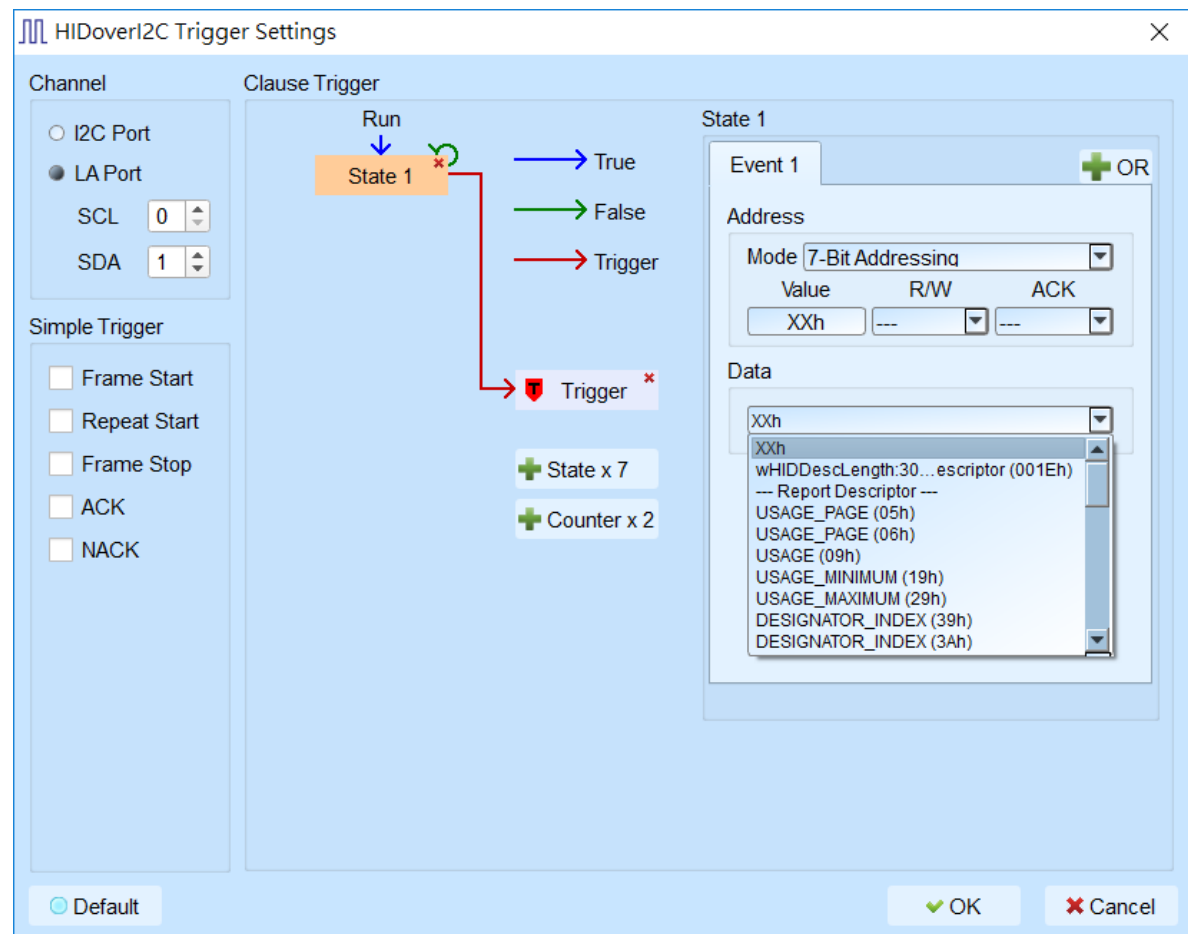
1. **Channel:** Select channels.
2. **Startup settings:** Set the initial parameters of eSPI.
3. **Trigger on:** Trigger specific error of eSPI.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Response fields, default value is 00h.

HIDoverI2C Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

HIDoverI2C Trigger Settings

Click HIDoverI2C Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select I2C / LA port.
2. **Simple Trigger:** Specific trigger function of I2C.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the R/W, ACK and Data(HID Descriptor) fields, default value is XX means “don’t care”.

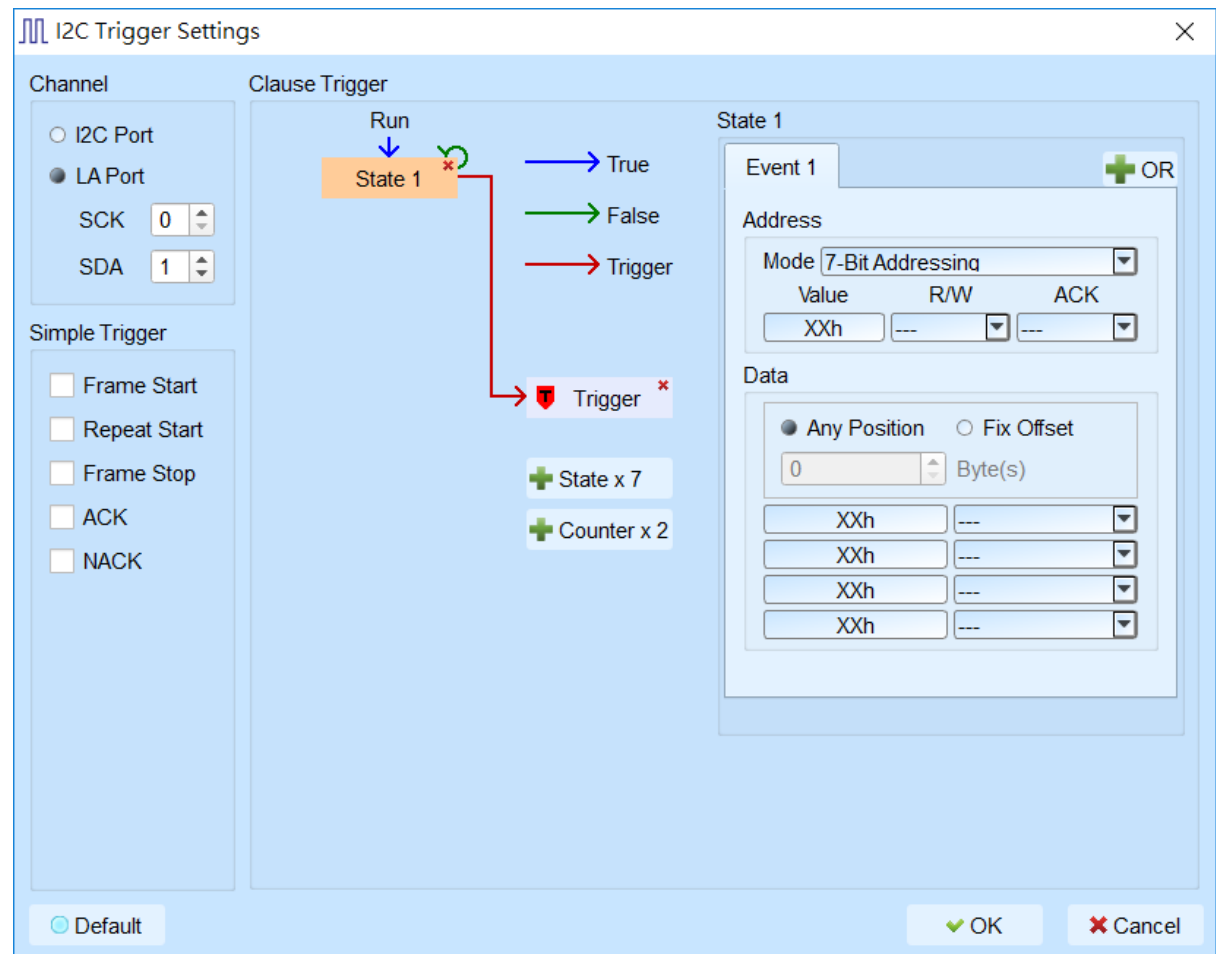
I²C Trigger

Supported Models : UPLA-1G17-16MP0. UPLA-1G34-1GP1. UPLA-1G34-1GP2.

UPLA-2G34-8GP3

I2C Trigger Settings

Click I2C Trigger in the toolbar and will show the dialog as the following.



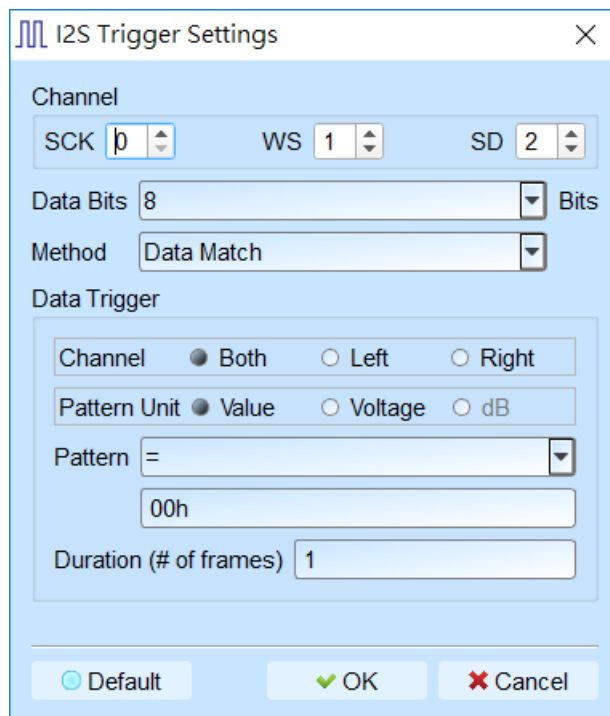
1. **Channel:** Select I2C / LA port.
2. **Simple Trigger:** Specific trigger function of I2C.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the R/W, ACK and Data fields, default value is XX means “don’t care”.

I²S Trigger

Supported Models : UPLA-1G34-1GP1.UPLA-1G34-1GP2. UPLA-2G34-8GP3

I2S Trigger Settings

Click I2S Trigger in the toolbar and will show the dialog as the following.



The image shows a software dialog box titled "I2S Trigger Settings". It contains several configuration fields: "Channel" with sub-fields for SCK (set to 0), WS (set to 1), and SD (set to 2); "Data Bits" set to 8; "Method" set to "Data Match"; and a "Data Trigger" section with radio buttons for "Both", "Left", and "Right" (all set to "Both"), "Pattern Unit" with radio buttons for "Value", "Voltage", and "dB" (all set to "Value"), a "Pattern" dropdown set to "=", a text field containing "00h", and a "Duration (# of frames)" text field set to "1". At the bottom are three buttons: "Default" (with a circular arrow icon), "OK" (with a green checkmark icon), and "Cancel" (with a red X icon).

1. **Channel:** Select Serial clock (SCK), word select (WS) and serial data (SD).

2. **Data Bits:** 1-32 bits, normally it is 8, 12, 16, 24 or 32.

3. **Method:**

Data Match : Trigger when the conditions matched.

Rising Edge : Trigger when it is a rising edge between two patterns.

Falling Edge : Trigger when it is a falling edge between two patterns.

Glitch : Trigger when there is a glitch.

Mute : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of $-P < X < +P$.

Clip : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of $-P < X \cup +P > X$.

Timing Violation : Provide 6 trigger conditions and this function will be enabled at 200 MHz sampling rate.

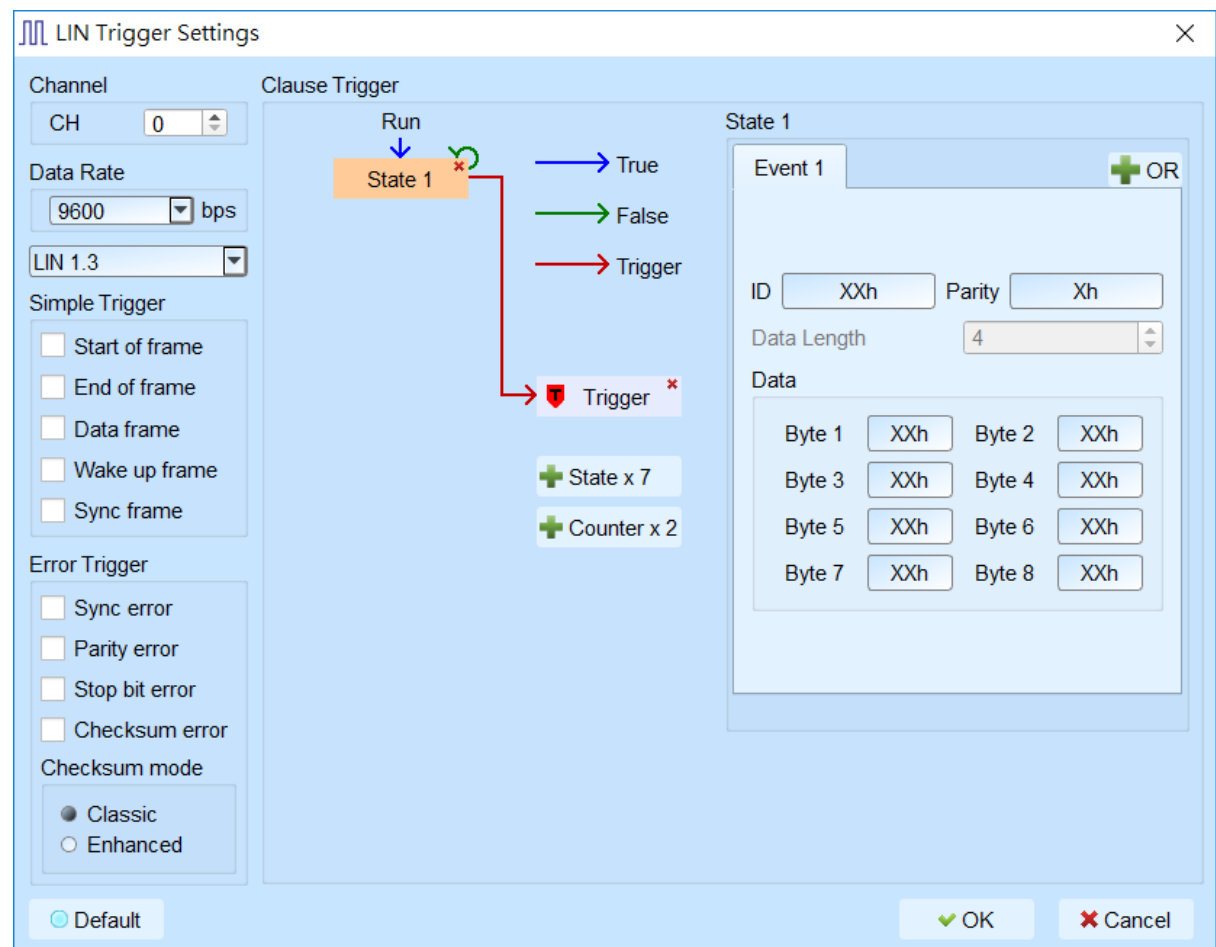
- 4. Data Trigger:** Select Both, Left, Right channel and pattern unit.

LIN Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

LIN Trigger Settings

Click LIN Trigger in the toolbar and will show the dialog as the following.



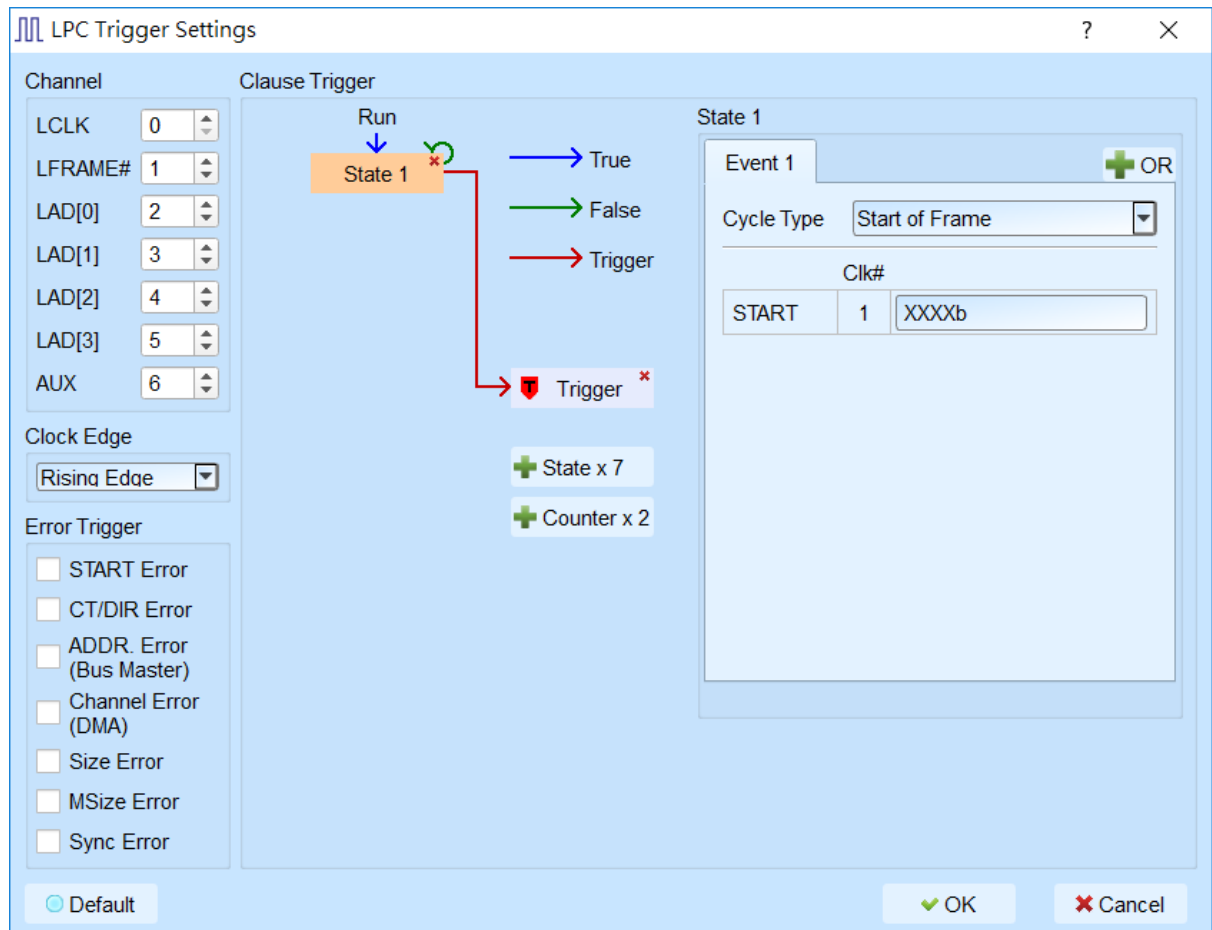
1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of LIN.
3. **Error Trigger:** Trigger specific error of LIN.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ID, Parity, Data Length and Data fields, default value is XX means “don’t care”.

LPC Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

LPC Trigger Settings

Click LPC Trigger in the toolbar and will show the dialog as the following.



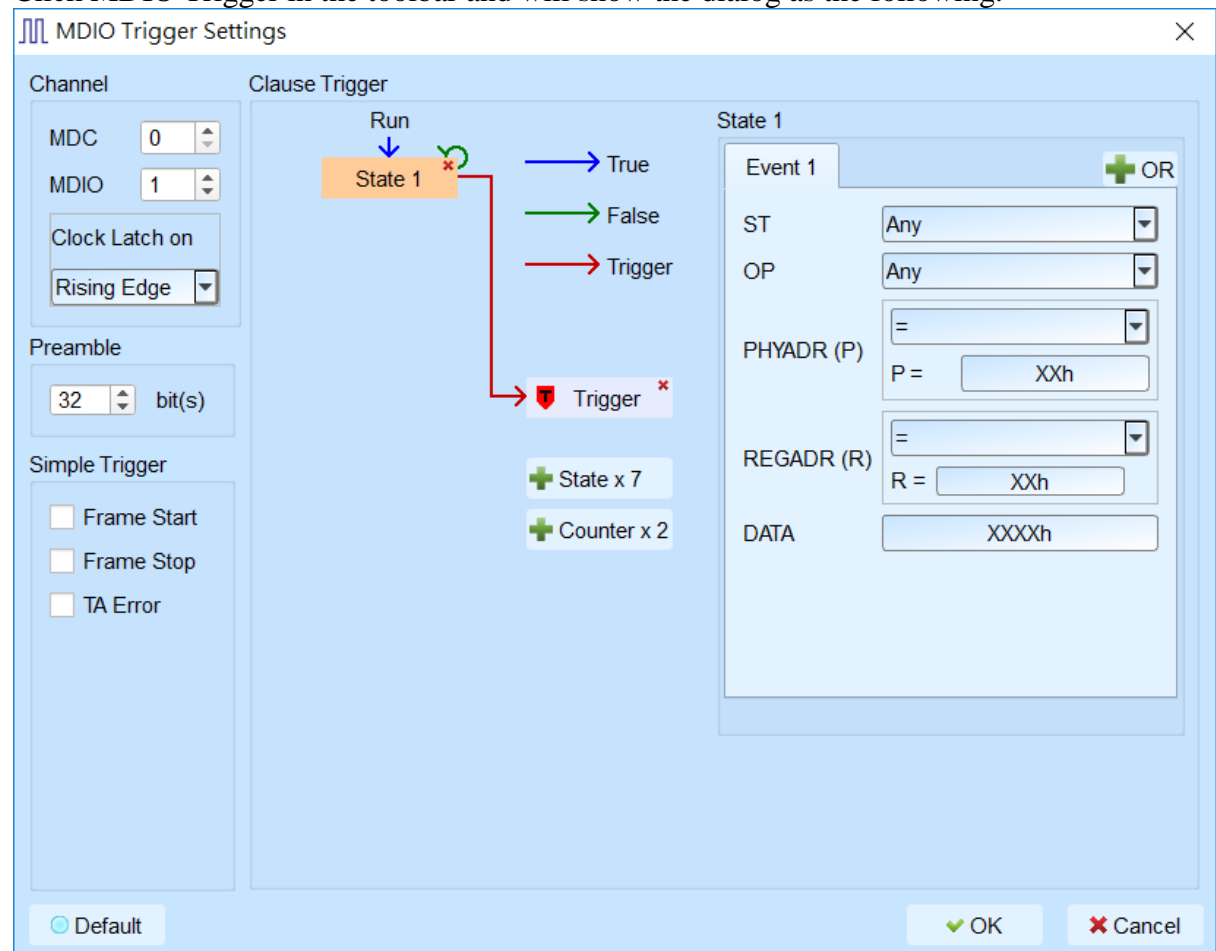
1. **Channel:** Select LPC channels.
2. **Clock Edge:** Select Rising/Falling clock edge.
3. **Error Trigger:** Trigger specific error of LPC.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Cycle Type and its parameters, default value is XX means “don’t care”.

MDIO Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

MDIO Trigger Settings

Click MDIO Trigger in the toolbar and will show the dialog as the following.



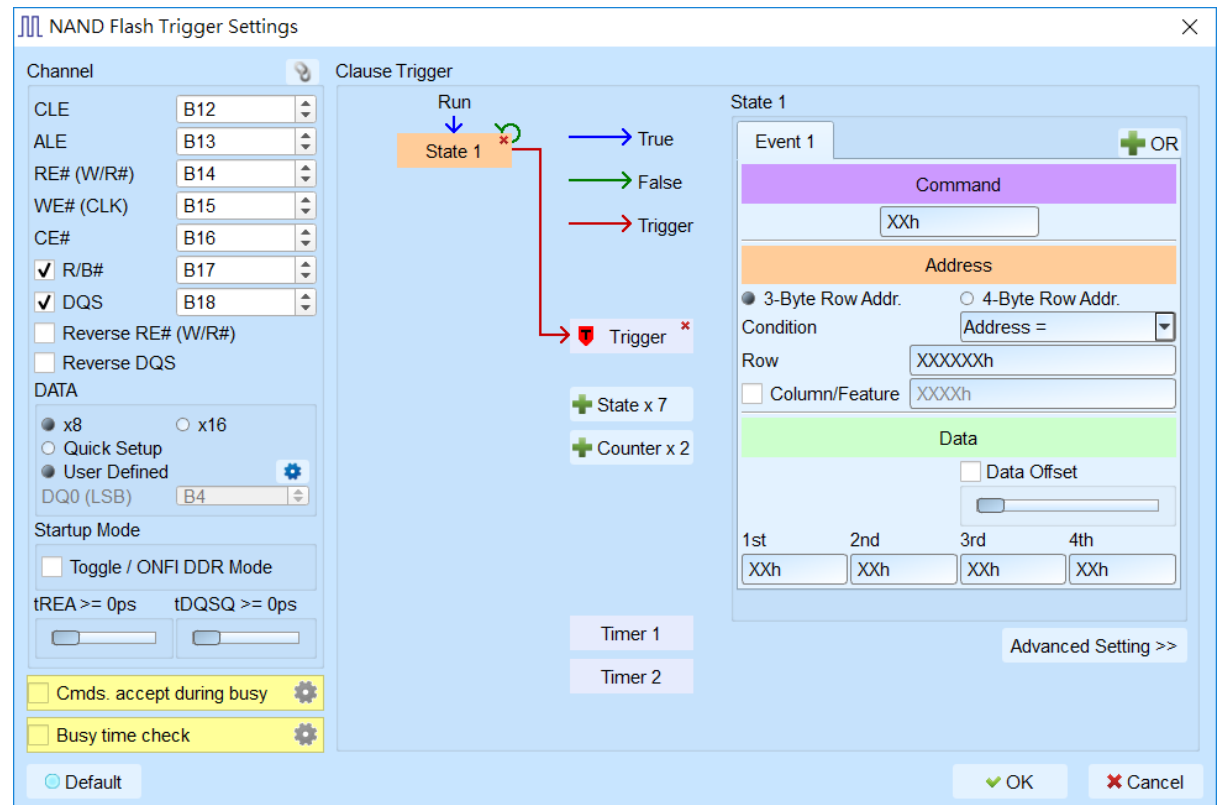
1. **Channel:** Select MDC / MDIO channels.
2. **Preamble:** Select the length of preamble.
3. **Simple Trigger:** Specific trigger function of MDIO.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ST, OP, PHYADR, REGADR and DATA fields, default value is XX means “don’t care”.

NAND Flash Trigger

Supported Models : UPLA-2G34-8GP3

NAND Flash Trigger Settings

Click NAND Flash Trigger in the toolbar and will show the dialog as the following.



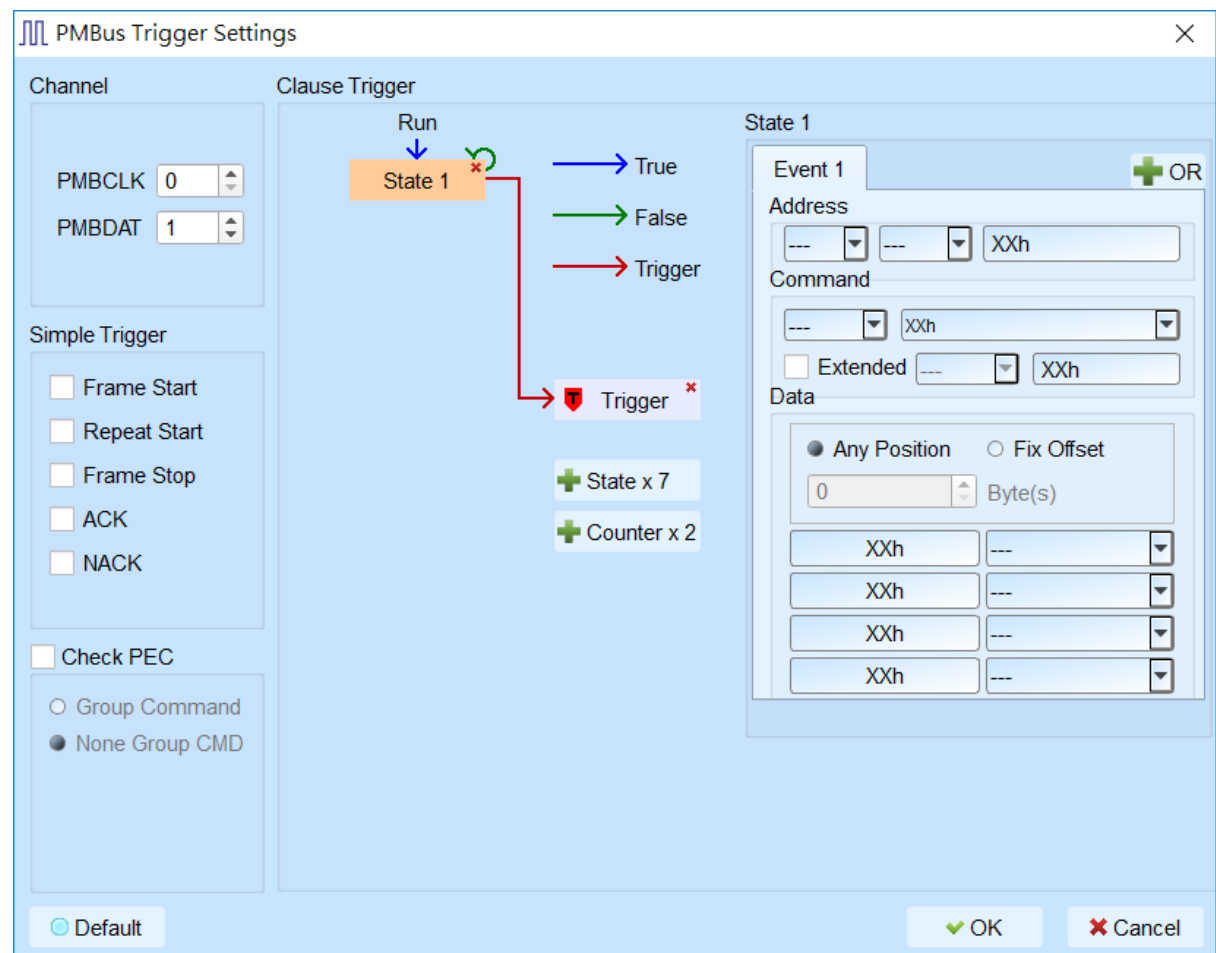
1. **Channel:** Select CLE, ALE, RE, WE, CE, R/B, DQS channels.
2. **DATA:** Select x8 or x16 bits
 - I. **Quick Setup:** Only set DQ0(LSB), others will be set automatically.
(e.g. LSB = B4, MSB = B11; LSB = B7, MSB = B14)
 - II. **User Defined:**

PMBus Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

PMBus Trigger Settings

Click PMBus Trigger in the toolbar and will show the dialog as the following.



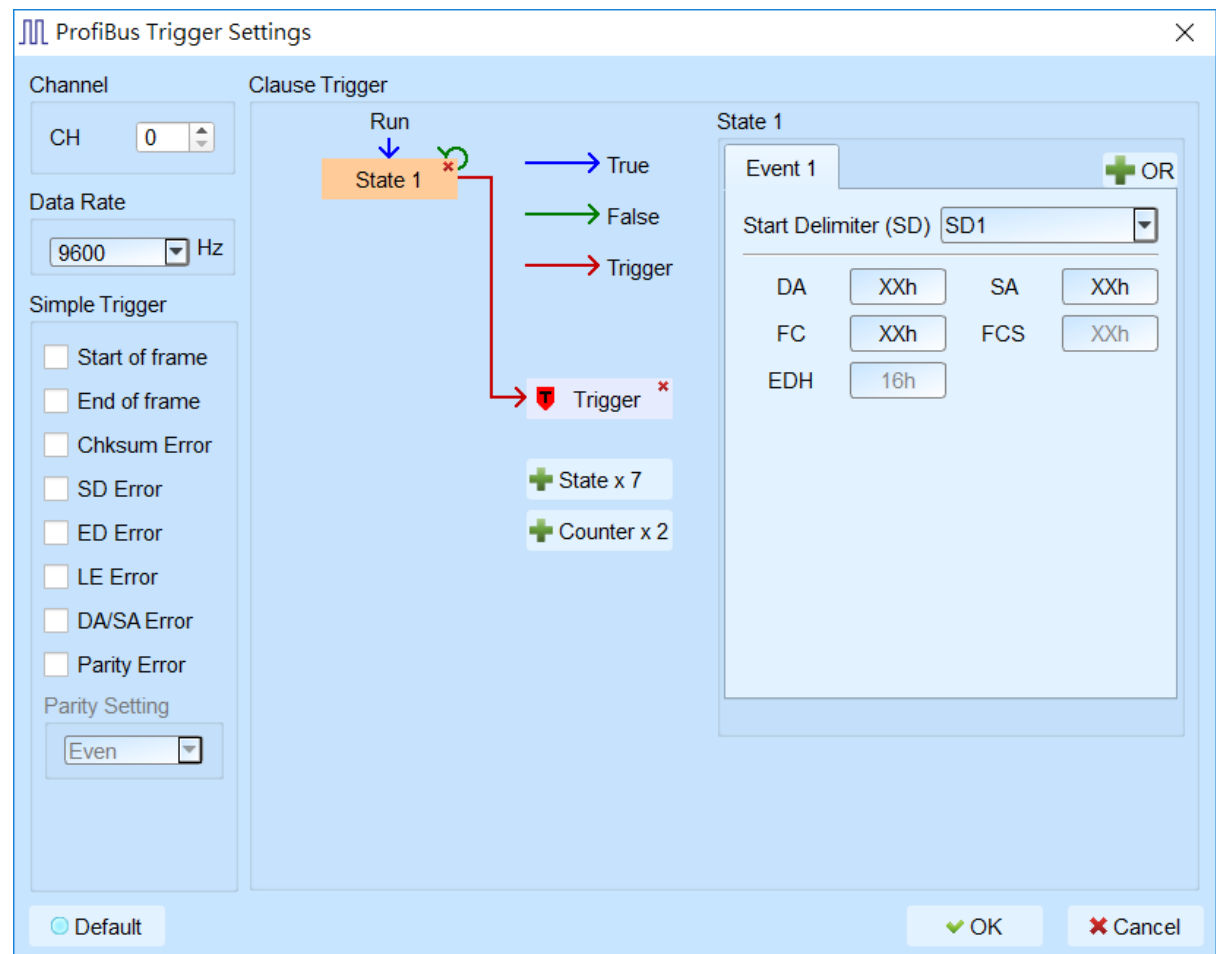
1. **Channel:** Select I2C / LA port.
2. **Simple Trigger:** Specific trigger function of I2C.
3. **Check PEC:** Trigger PEC.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command and Data fields, default value is XX means “don’t care”.

ProfiBus Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

ProfiBus Trigger Settings

Click ProfiBus Trigger in the toolbar and will show the dialog as the following.



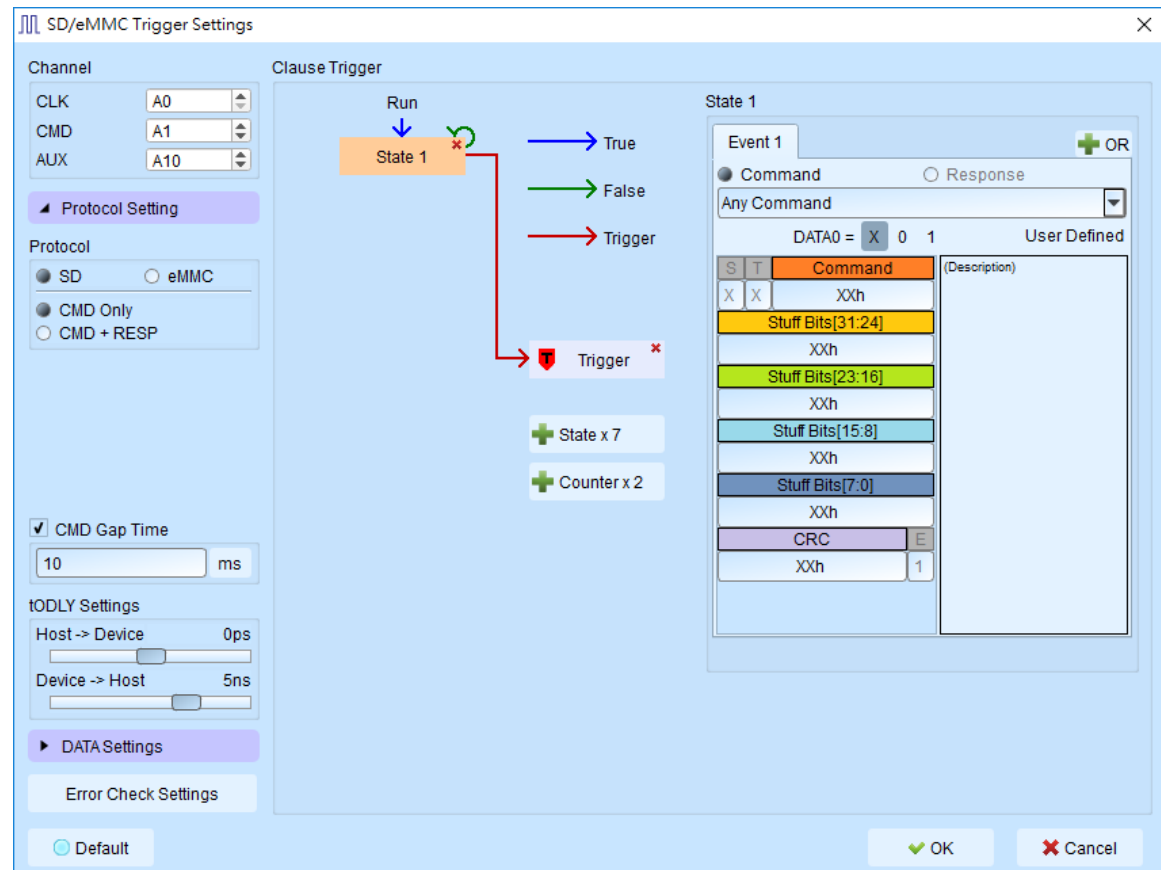
1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of ProfiBus.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SD packet and its fields, default value is XX means “don’t care”.

SD/eMMC Trigger

Supported Models : UPLA-2G34-8GP3

SD/eMMC Trigger Settings

Click **SD/eMMC Trigger** in the toolbar and will show the dialog as the following ◦



1. **Channel:** select CLK, CMD and AUX as the trigger channel.
2. **Protocol:** select SD or eMMC trigger
3. **CMD Gap time:** delay trigger between the two CMDs.
4. **tODLY Settings:** set the phase delay time such that the device can latch valid command and response.
5. **Clause trigger settings:** Please reference Clause Trigger chapter
6. **Trigger settings**

SD/eMMC decoder

The screenshot shows the 'Event 1' configuration window. It has a tabbed interface with 'Event 1' selected. Below the tabs, there are radio buttons for 'Command' (selected) and 'Response'. A dropdown menu shows 'Any Command'. Below this, there is a 'DATA0' field with a value of 'X' and a 'User Defined' checkbox. The main area contains a table with columns 'S', 'T', and 'Command'. The table has several rows: 'Command' (XXh), 'Stuff Bits[31:24]' (XXh), 'Stuff Bits[23:16]' (XXh), 'Stuff Bits[15:8]' (XXh), 'Stuff Bits[7:0]' (XXh), 'CRC' (XXh), and 'CRC' (XXh). The 'CRC' row has a value of '1' in the 'T' column. The 'Command' column has a value of 'XXh' for the first row. The 'Description' column is empty.

S	T	Command	(Description)
X	X	XXh	
		Stuff Bits[31:24]	
		XXh	
		Stuff Bits[23:16]	
		XXh	
		Stuff Bits[15:8]	
		XXh	
		Stuff Bits[7:0]	
		XXh	
		CRC	
		XXh	

Parameter :

DATA0 = X 0 1 : use Data0 to judge the R1 and R1b.

Input trigger value, input 'X' means don't care.

Append 'h' for HEX, 'b' for binary, no append for DEC.

When cursor on the input table, the information showed in the right side field.

User Defined add the command reserved:

The screenshot shows the 'User Defined Command Setting' dialog box. It has a title bar with a close button. The main area contains a table with columns 'Command' and 'Description'. The table has several rows: 'Cmd 1', 'Cmd 5', 'Cmd 14', 'Cmd 21', 'Cmd 22', 'Cmd 26', 'Cmd 31', and 'Cmd 34'. Each row has a 'Click To Edit...' button in the 'Description' column. At the bottom, there are buttons for 'Reset All', 'OK', and 'Cancel'.

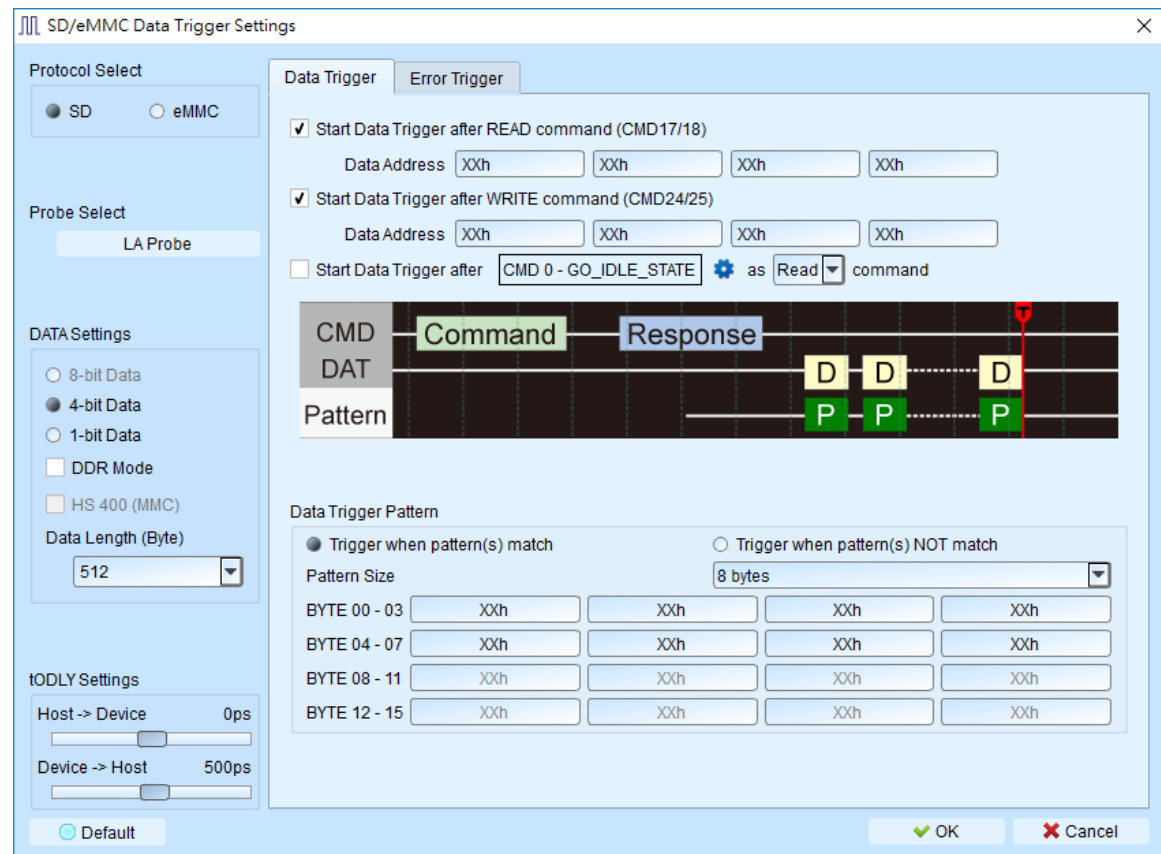
Command	Description
Cmd 1	Click To Edit...
Cmd 5	Click To Edit...
Cmd 14	Click To Edit...
Cmd 21	Click To Edit...
Cmd 22	Click To Edit...
Cmd 26	Click To Edit...
Cmd 31	Click To Edit...
Cmd 34	Click To Edit...

SD/eMMC Data Trigger

Supported Models : UPLA-2G34-8GP3

SD/eMMC Data Trigger Settings

Click **SD/eMMC Data Trigger** in the toolbar and will show the dialog as the following °



1. **Protocol:** select SD or eMMC trigger
2. **Probe Select:** select CLK, CMD and AUX as the trigger channel.
3. **Data Settings:** select current bus width, byte, SDR, DDR of the test object
4. **tODLY Settings:** set the phase delay time such that the device can latch valid command and response.
5. **Data Trigger:** set the patterns of data trigger.

SD/eMMC Data Trigger Settings

Protocol Select

SD

eMMC

Probe Select

LA Probe

DATA Settings

8-bit Data

4-bit Data

1-bit Data

DDR Mode

HS 400 (MMC)

Data Length (Byte)

512

TODLY Settings

Host -> Device

0ps

Device -> Host

500ps

Default

Data Trigger

Error Trigger

Trigger on Data IDLE timeout after CRC status

CMD

Time

DAT

Data

CRC Status

Trigger when IDLE time > 5 ms

Trigger on Data IDLE timeout after CMD

CMD

Host Command

Card Response

Time

DAT

Data

CMD Lists

Cmd 17

Cmd 18

Cmd 24

Cmd 25

Trigger when IDLE time > 5 ms

OK

Cancel

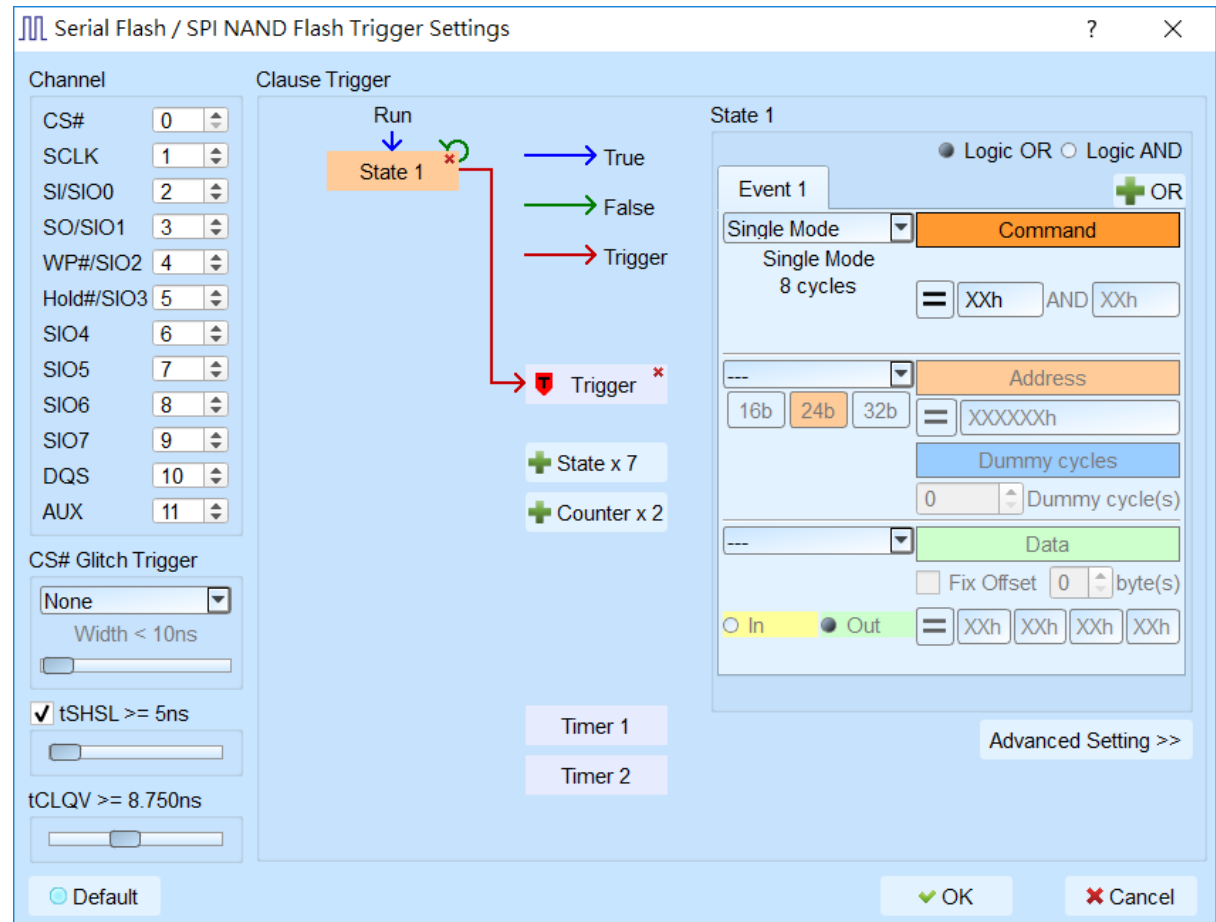
6. **Error Trigger:** set the condition of idle time to trigger.

Serial Flash / SPI NAND Trigger

Supported Models : UPLA-2G34-8GP3

Serial Flash / SPI NAND Flash Trigger Settings

Click Serial Flash Trigger in the toolbar and will show the dialog as the following.



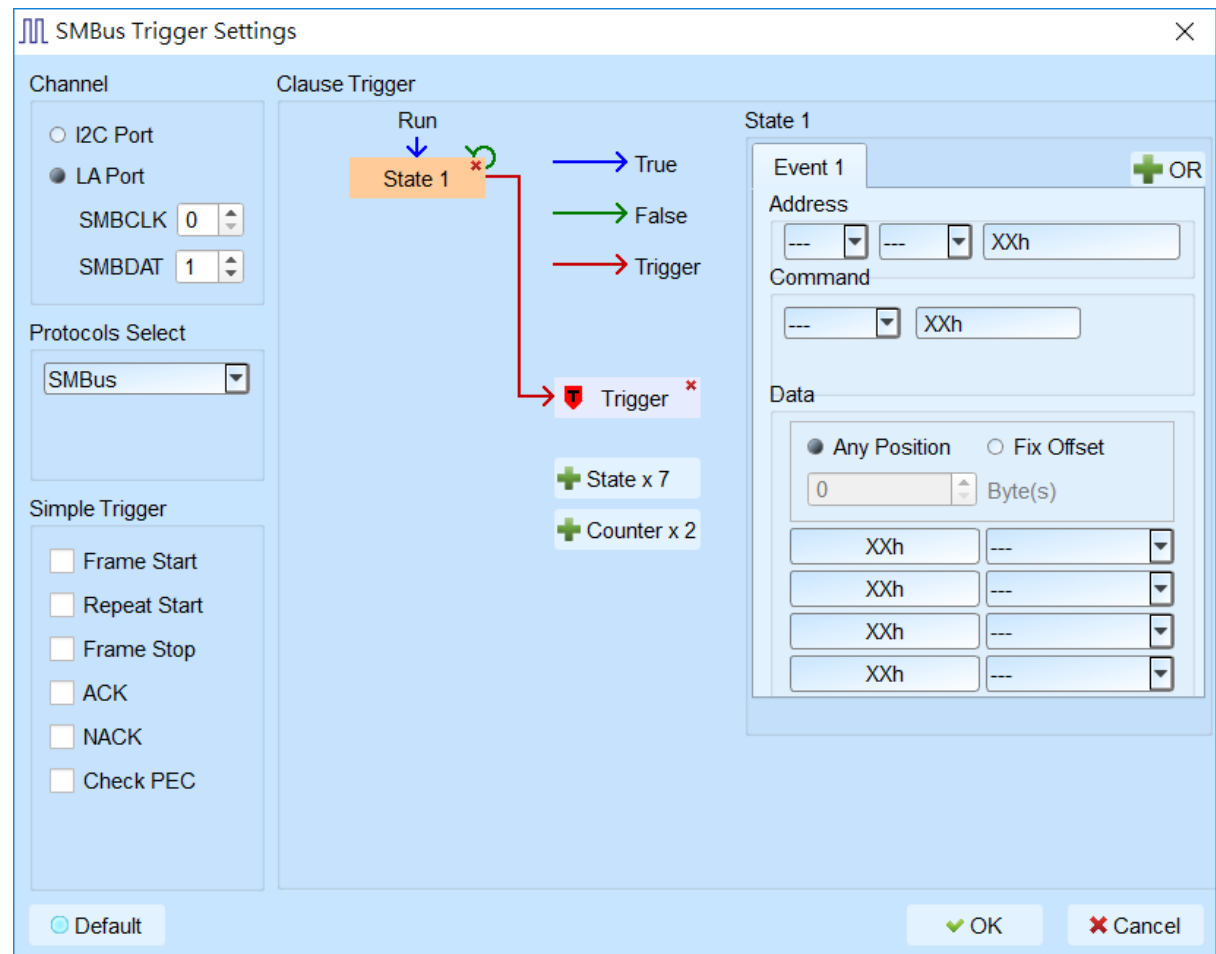
1. **Channel:** Select channels.
2. **CS# Glitch Trigger:** Trigger the glitch on CS# channel.
3. **tSHSL / tCLQV:** Set tSHSL / tCLQV.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Command, Address and Data fields, default value is XX means "don't care".

SMBus Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

SMBus Trigger Settings

Click SMBus Trigger in the toolbar and will show the dialog as the following.



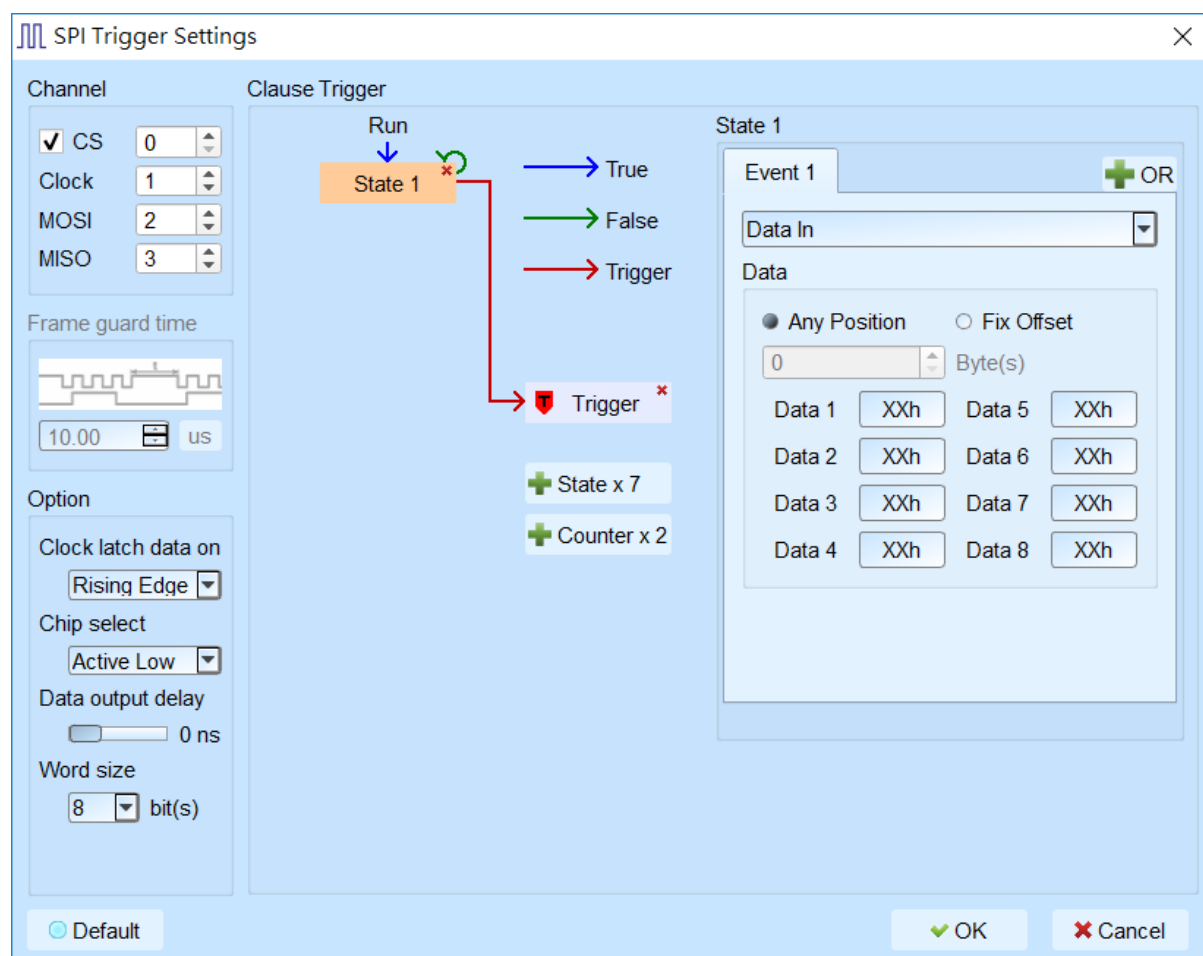
1. **Channel:** Select I2C / LA port.
2. **Protocols Select:** Select SMBus / SBS / SPD protocol.
3. **Simple Trigger:** Specific trigger function of SMBus.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command and Data fields, default value is XX means “don’t care”.

SPI Trigger

Supported Models : UPLA-1G34-1GP1. UPLA-1G34-1GP2. UPLA-2G34-8GP3

SPI Trigger Settings

Click SPI Trigger in the toolbar and will show the dialog as the following.



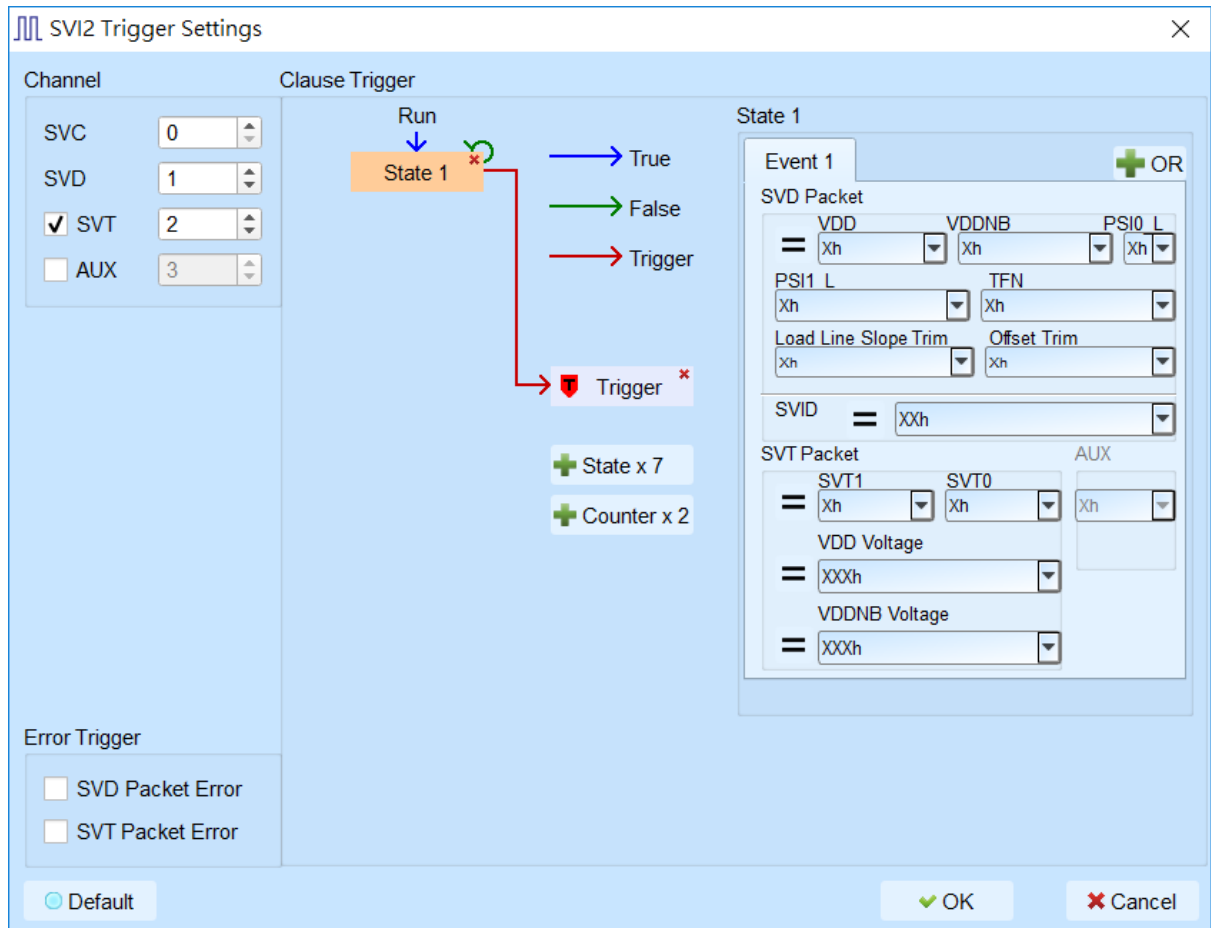
1. **Channel:** Select SPI channels.
2. **Frame guard time:** Only for unchecked CS state.
3. **Option:** Set SPI parameters.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Data fields, default value is XX means “don’t care”.

SVI2 Trigger

Supported Models : UPLA-1G34-1GP2.UPLA-2G34-8GP3

SVI2 Trigger Settings

Click SVI2 Trigger in the toolbar and will show the dialog as the following.



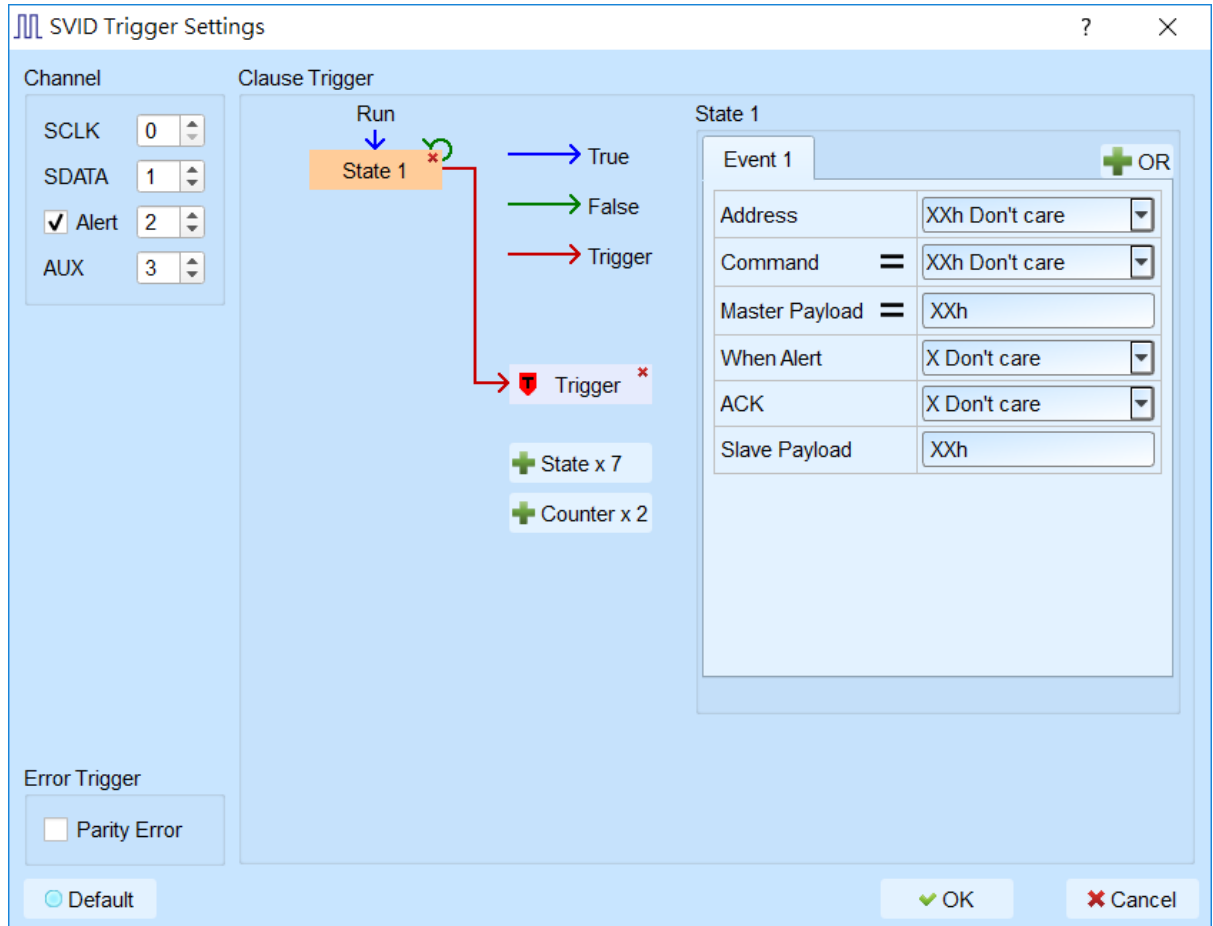
1. **Channel:** Select channels.
2. **Error Trigger:** Trigger specific error of SVI2.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SVD and SVT packet, default value is XX means “don’t care”.

SVID Trigger

Supported Models : UPLA-1G34-1GP2.UPLA-2G34-8GP3

SVID Trigger Settings

Click SVID Trigger in the toolbar and will show the dialog as the following.



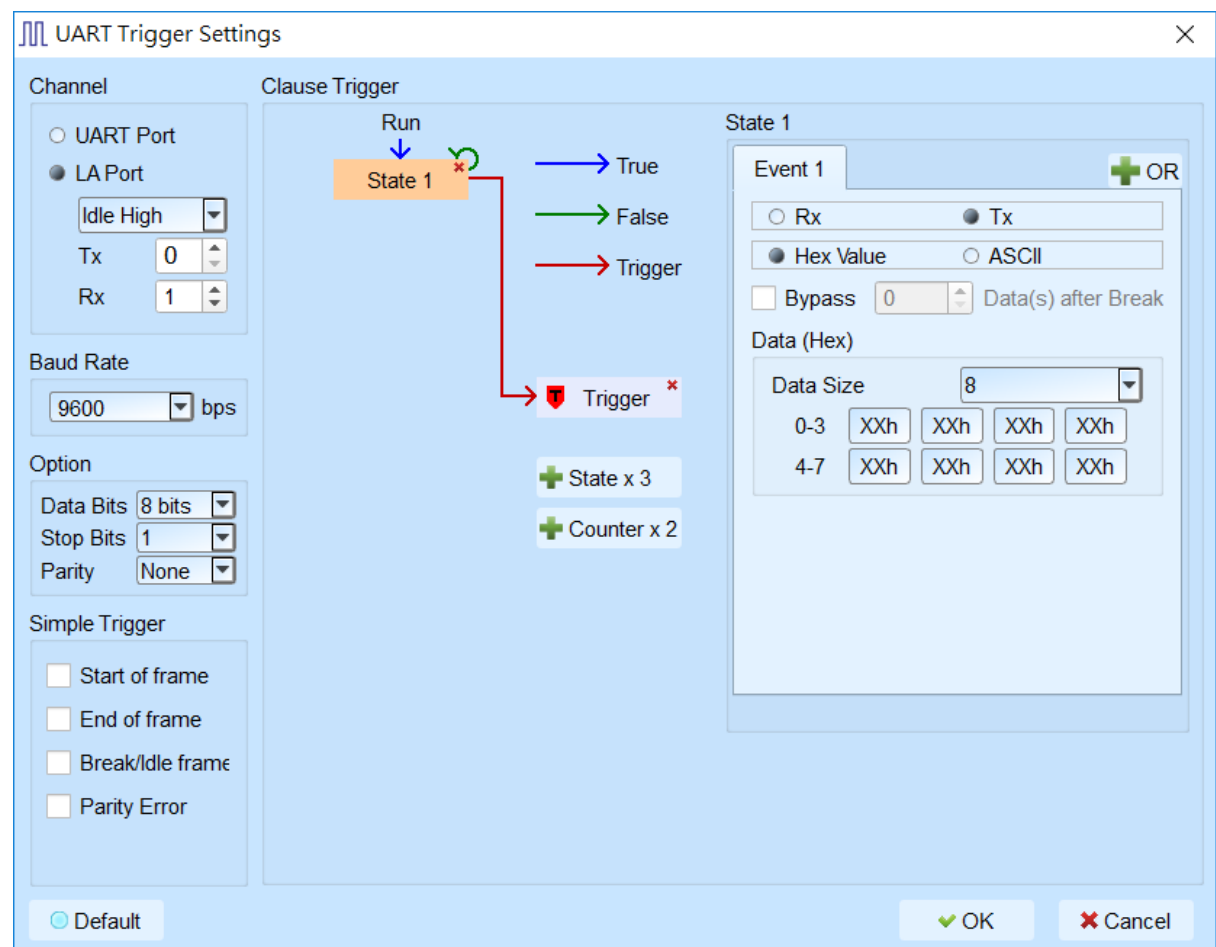
1. **Channel:** Select channels.
2. **Error Trigger:** Set SVID Parity Error trigger.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command, Master Payload, ACK and Slave Payload fields, default value is XX means “don’t care”.

UART Trigger

Supported Models : UPLA-1G34-1GP1. UPLA-1G34-1GP2. UPLA-2G34-8GP3

UART Trigger Settings

Click UART Trigger in the toolbar and will show the dialog as the following.



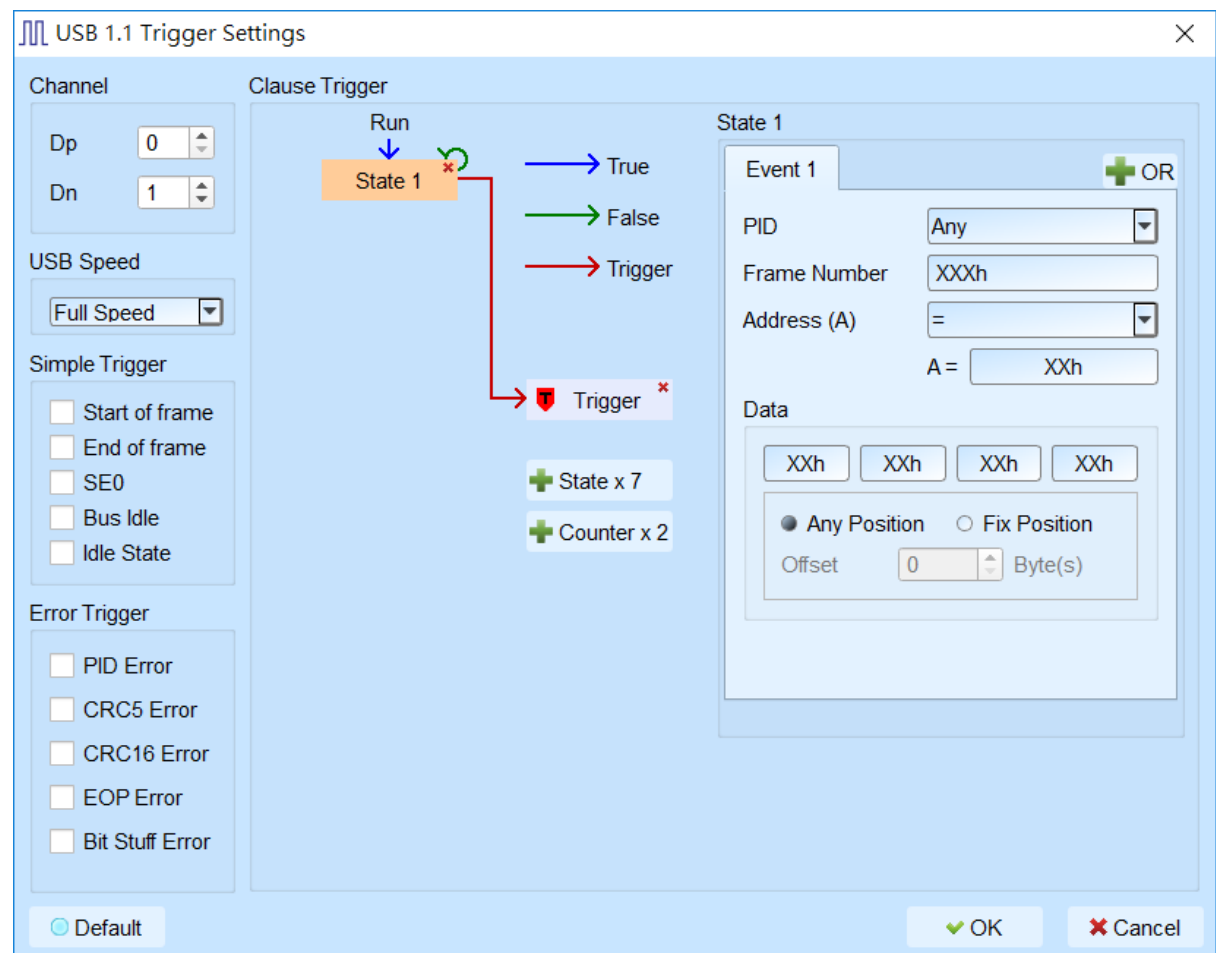
1. **Baud Rate:** Select UART baud rate.
2. **Simple Trigger:** Specific trigger function of UART.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing the trigger values in the Data fields, default value is XX means “don’t care”.

USB1.1 Trigger

Supported Models : UPLA-1G34-1GP2. UPLA-2G34-8GP3

USB 1.1 Trigger Settings

Click USB 1.1 Trigger in the toolbar and will show the dialog as the following.



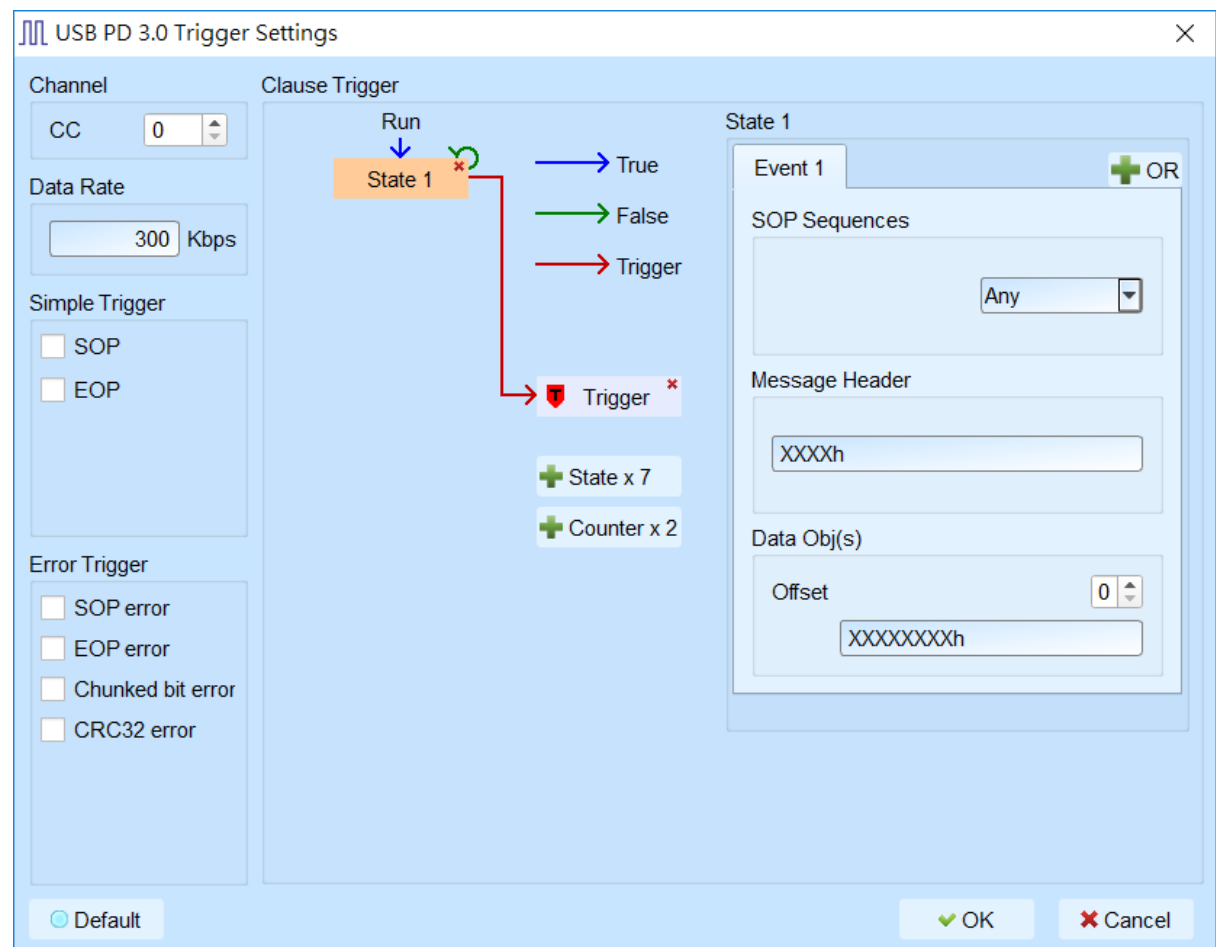
1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of USB 1.1.
3. **Error Trigger:** Trigger specific error of USB 1.1.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the PID, Frame Number, Address and Data Field, default value is XX means “don’t care”.

USB PD 3.0 Trigger

Supported Models : UPLA-1G34-1GP2.UPLA-2G34-8GP3

USB PD 3.0 Trigger Settings

Click USB PD 3.0 Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of USB PD 3.0.
3. **Error Trigger:** Trigger specific error of USB PD 3.0.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SOP Sequences, Message Header and Data Obj(s), default value is XX means “don’t care”.